ECE 327: *Electronic Devices and Circuits Laboratory I*

Procedure for Lab 6 (Digital-to-Analog Conversion (DAC) Lab)

SEE LAB *BOOK*. The questions you must answer **in your report** are given in the book.

Regulated power supply: **BY NOW**, you should be using a $10\,V_{DC}$ regulated supply for the *TRANSMITTER*. You **ALSO** need one for your *RECEIVER*. See the supplementary text for details. To ensure good performance, pay attention to bypass capacitors.

Bypass capacitors: Unless otherwise noted, **bypass capacitors** terminate at $0\,V_{DC}$.

Construction: **YOU WILL KEEP EVERYTHING** that you build in this laboratory. Build your circuits to be **clean**, **accessible**, and **COMPACT**. **TRY TO BUILD ENTIRE RECEIVER IN *SAME* BREADBOARD "*COLUMN*."** Be sure to make the ***PWM demodulator output*** *EASY TO FIND* in later laboratories.

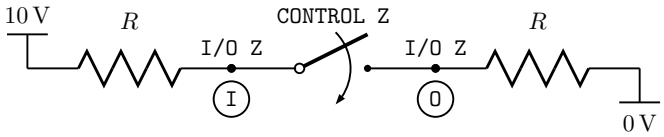
REPORT: You do NOT need to report on the nonpositive steps of the procedure.

-2. Build a ***second*** $10\,V_{DC}$ LM317 voltage regulator for your **RECEIVER** (i.e., your PWM demodulator).

- See supplementary text for details.
- Use $\sim 0.1\,\mu$F bypass capacitor at $15\,V_{DC}$ input *near* input pin.
- Use $\sim 1\,\mu$F bypass capacitor at $10\,V_{DC}$ output (across rails is fine).
  - A $.47\,\mu$F **bypass capacitor** *near* components across each breadboard rail will be sufficient.
  - An additional $\sim 1\,\mu$F bypass capacitor at the Adjust pin is a good idea.
- **ISOLATE** a set of supply rails for your receiver.
  - Your transmitter and receiver my share **ground** rails but **SHOULD NOT** share 10 V rails.
  - **FROM NOW ON**, use *receiver* supply rails (**except** for the infrared LED).

-1. This lab requires **THREE** FET analog switches. Use one or more CD4066 parts for these switches—**TEST SWITCHES BEFORE** continuing.

- Construct the testing circuit shown below. Use $R = 1\,k\Omega$ and connect $V_{DD} = 10\,V$ and $V_{SS} = 0\,V$.



CONTROL	⟹	I	O
0 V	⟹	10 V	0 V
10 V	⟹	5 V	5 V

- When you connect CONTROL to 0 V or 10 V, **use a $1\,k\Omega$ resistor** (for safety).
- For 0 V *control*, use DMM to verify switch *input* sees 10 V and switch *output* sees 0 V.
- For 10 V *control*, use DMM to verify *input* **and** *output* ***BOTH*** see ***the same*** 5 V.
- **TEMPORARILY** connect control to 30 kHz clock and verify **no switch delay**.
- Repeat until you find **THREE** working switches.
- **DISCONNECT switch testing circuit.** You may leave V_{DD} and V_{SS} connected.

0. This lab requires **TWO** CMOS inverters. Find them on a CD4049—**TEST INVERTERS BEFORE CONTINUING**

- Connect V_{DD} to 10 V and V_{SS} to 0 V.
- Using a $1\,k\Omega$ resistor (for safety), connect inverter input to 10 V; use DMM to verify 0 V output.
- **RE**connect $1\,k\Omega$ resistor at inverter input to 0 V; use DMM to verify 10 V output.
- Connect inverter input to 30 kHz 555 clock and use oscilloscope to verify output is correct.
- Repeat until you find **TWO** working inverters.
- **DISCONNECT** inverter inputs that were used for testing.

1. Design, build, and test your infrared (IR) link (see **Figure 6.2** from book).

   (i) Complete your **transmitter** by building the **current driver** for the QEE113 infrared LED.
   - Choose **one** of the **four** circuits from the supplementary text to drive ∼40 mA into the LED.
     - If using an *npn*-style driver, **wire input** to your PWM modulator flip–flop's Q output.
     - If using a *pnp*-style driver, **wire input** to your PWM modulator flip–flop's $\overline{Q}$ output.
   - **IF POSSIBLE**, use old **TRANSMITTER** 10 V supply rail.
   - Try **NOT** to use LED to bridge a DIP gap on your breadboard.
     - Wiring *parallel* to gap will make it easier to place receiver.
   - Do **NOT** use a POTENTIOMER for the series resistor (i.e., use discrete 220 Ω instead).
     - Tuning *distances* will be more effective.

   (ii) Install a QSE157 infrared receiver.
   - **DO NOT** install a pull-up resistor!! It has a fast totem-pole output!
   - Install receiver so that it **faces** transmitter.
     - Ideally, you can separate the two by up to ∼0.5 m.
   - **IF POSSIBLE**, use *new* **RECEIVER** 10 V supply rail.
   - *OPTIONAL*: Use ∼0.1 μF **bypass capacitor** *near the part* from V_{CC} to ground.

   (iii) **TEST** and **TUNE** the IR link.

   NOTE: The transmitted light is **INFRARED**, which is **OUTSIDE OF THE VISIBLE SPECTRUM**. You **WILL NOT** be able to see the light!

   - **Temporarily** disconnect the **LSA output** from the **PWM input** (i.e., inverting ("–") input of LM311 comparator).
   - Apply 2 V_{DC} to the PWM input.
     - Use your second DC supply output **OR** the middle pin of a potentiometer stretched across 0 V and 10 V.
       - CONNECT (i.e., do NOT use a probe!) your digital multimeter (DMM) to measure the *actual* input voltage.
       - Remember that your DMM ground can be connected to your common ground with a banana connector.
     - Plot IR link input and output on oscilloscope.
       - **Channel 1**: PWM output
       - **Channel 2**: QSE157 receiver output
       - Set **trigger** `Edge` to **rising** transitions on source `1`.
         - Adjust **trigger level knob** or **trigger filtering** (see `Mode`) until display stabilizes.
       - Use `Quick Meas` to show `+ Width` of source `1`.
       - Use `Quick Meas` to show `– Width` of source `2`.
       - **Output** should look like **inverted** version of **input**.
       - `TUNE` **transmitter current** (i.e., R_L) and/or **transmitter–receiver DISTANCE** until widths differ 0.9 μs or less.
         - Adjusting R_L value *can* help.
         - SLIGHT adjustments of **DISTANCE** will make the MOST IMPACT.
         - To reduce impact of infrared noise from above, AVOID tilting the receiver upward.
   - Apply 8 V_{DC} to the PWM input.
     - Verify that transmitted and received pulses differ by no more than 0.9 μs.
   - **SAVE A PLOT** showing input `+ Width` and output `– Width` for 2 V_{DC} PWM input.
   - **SAVE A PLOT** showing input `+ Width` and output `– Width` for 8 V_{DC} PWM input.

2. Build, test, and tune the ramp generator.

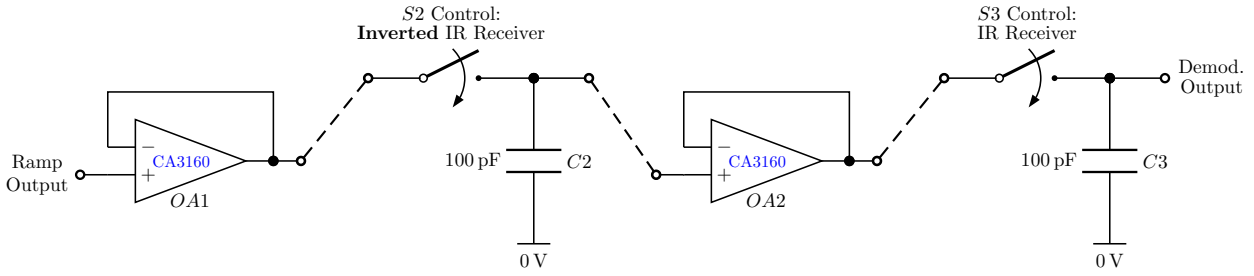
   (i) As before, apply 8 V_{DC} to PWM input.

   (ii) Connect QSE157 (IR receiver) output to the input of **one of the two** working CD4049 inverters.
   - *OPTIONAL:* Place ~0.1μF **bypass capacitor** *near the part* from inverter V_{DD} to ground.
   - View inverter **input** and **output** on same oscilloscope screen to verify correct operation.
     - The result is an inverted version of the IR receiver signal.
   - **MARK OUTPUT NODE**. You will use it later.

   (iii) Connect **this inverter output** to the ***other* working inverter's input** on the CD4049.
   - *OPTIONAL:* Place ~0.1μF **bypass capacitor** *near the part* from inverter V_{DD} to ground.
   - View *SECOND* inverter **input** and **output** on same screen to verify correct operation.
     - The result should look nearly identical to the IR receiver signal.
     - This second inverter produces a ***SLIGHTLY* delayed** version of the IR receiver signal.

   (iv) Choose a ramp generator from the supplementary text.
   - Regardless of your ADC lab choice, the **resistor-biased** option is easiest to tune in this lab!
   - Make **SURE** you use **RECEIVER**'s 10 V supply for **ENTIRE** ramp circuit. Don't mix!
   - Design to have the **SAME SLOPE** as your ADC generator (i.e., ~0.32 V/μs).
     - For the resistor-biased option, try choosing $v_B = 9$ V and $R_E = 470\,\Omega$.
       * You will *tune* v_B later so that ramp slopes match. **No math** is required here!
     - Use the same C that you used for the ADC lab's ramp generator (usually $C = 2.2$ nF).
       * In **Figure 6.3** from book, this capacitor is $C1$.
   - For tuning, implement the R_1–R_2 divider (or the R_E resistor) with a POTENTIOMETER.
   - Use **one of the three CD4066 switches** that you tested above.
     - In **Figure 6.3** from book, this CD4066 switch is $S1$ with control $SC1$.
   - Connect **SECOND inverter output** to **ramp generator reset** (CD4066 control input).
     - That is, connect **delayed IR receiver** to CD4066 **switch control** $SC1$**.**
   - **TEST and TUNE** your ramp generator.
     - Plot **transmitter ramp** on oscilloscope **channel** `1`.
     - Plot **receiver ramp** on oscilloscope **channel** `2`.
     - Set **trigger** `Edge` for **rising** transitions on **channel** `1`.
       * Adjust **level** or **filtering** (see `Mode`) to stabilize display.
     - If necessary, turn on `Averaging` under `Acquire` where `# Samples` is set to `1`.
     - Adjust **horizontal** and **vertical** scales to zoom in on one ramp.
       * USE **SAME VERTICAL SCALE** (e.g., 2 V/div) on BOTH CHANNELS!!
     - **`Tune` NEW RECEIVER RAMP** slope until ramps are **parallel**.
       * For example, try align so that ramps *overlap*. After tuning, they should be be *colinear*.
   - *OPTIONAL*: To *prevent switching noise*, place **small (ceramic) bypass capacitor** (e.g., 0.1 μF) from supply pin (i.e., 10 V_{DC} input) to ground.

   (v) Plot **transmitter ramp** and **receiver ramp** on same oscilloscope screen.
   - Set **trigger** `Edge` for **rising** transitions on either channel.
     - Adjust **level** or **filtering** (see `Mode`) to stabilize display.
   - MANUALLY vary PWM input from 2 V_{DC} to 8 V_{DC}.
     - Tops of ramps should approximately track DC input. Slopes should ALWAYS be parallel.
   - Do the ramps start rising at the same time? **WHY NOT?**
   - **SAVE A PLOT** of the ramps (separate on screen if necessary).



(i) Ramp buffer (ii) Ramp S&H (iii) S&H Buffer (iv) Output S&H

3. Construct and test the remainder of the demodulator (i.e., build the "analog D flip–flop" ramp sampler)

   (i) Construct ramp **buffer** (i.e., unity-gain non-inverting OA configuration like (i)).
   - Use CA3160 operational amplifier (fast and has **very low leakage**).
     - If none available, use CA3130 with 45–100 pF (e.g., 68 pF) from pin 1 to pin 8.
     - Operational amplifier is $OA1$ in **Figure 6.2** from book.
     - *OPTIONAL:* Place ∼0.1μF **bypass capacitor** from $V+$ (i.e., *at* supply pin) to ground.
   - Connect ramp to buffer input.
     - Buffer input is non-inverting (i.e., "+") input of operational amplifier.

   (ii) Construct **sample-and-hold circuit** (i.e., switch and capacitor like (ii)).
   - Connect sample-and-hold input to ramp buffer output.
   - Use **one of the three CD4066 switches** that you tested above.
     - In **Figure 6.3** from book, CD4066 switch is $S2$ with control $SC2$.
     - Connect CD4066 control to output of FIRST inverter (i.e., **inverted** IR receiver output).
   - Use 100 pF capacitor (capacitor is $C2$ from **Figure 6.2** from book). **Why** so small?

   (iii) Construct sample-and-hold **buffer** (i.e., unity-gain non-inverting OA configuration like (iii)).
   - Use CA3160 operational amplifier (fast and has **very low leakage**).
     - If none available, use CA3130 with 45–100 pF (e.g., 68 pF) from pin 1 to pin 8.
     - Operational amplifier is $OA2$ in **Figure 6.2** from book.
     - *OPTIONAL:* Place ∼0.1μF **bypass capacitor** from $V+$ (i.e., *at* supply pin) to ground.
   - Connect sample-and-hold output to buffer input.
     - Buffer input is non-inverting (i.e., "+") input of operational amplifier.

   (iv) Construct second **sample-and-hold circuit** (i.e., switch and capacitor like (iv)).
   - Connect sample-and-hold input to ramp buffer output.
   - Use **one of the three CD4066 switches** that you tested above.
     - In **Figure 6.3** from book, CD4066 switch is $S3$ with control $SC3$.
     - Connect CD4066 control to **IR receiver output.**
   - Use 100 pF capacitor (capacitor is $C3$ from **Figure 6.2** from book). **Why** so small?
   - **Demodulator output** is capacitor voltage. **MARK IT FOR EASY ACCESS**.

   ⊛ **TEST** pulse-width demodulator.
   - Plot **demodulator output** (i.e., $C3$ voltage) on oscilloscope. DO NOT AUTOSCALE!
     - **DO NOT** press `Autoscale`
     - Set **VERTICAL SCALE** to 2 V/div and **HORIZONTAL SCALE** to 20 μs/div.
     - **ALIGN** channel ground to **lowest grid line** on screen.
   - **YOU SHOULD SEE** a *horizontal line* that approximately matches the DC PWM input.
     - Press `Single` to view "chattering."
     - Chattering on output is due capacitor and *oscilloscope* **leakages**. Why?
     - The oscilloscope has a 10 MΩ input impedance, and the CA3160 has less than 5 pA of input leakage. Which load is a bigger drain on the 100 pF sample-and-hold capacitors?
   - **VARY** PWM input from 2 V_{DC} to 8 V_{DC}. Demodulator output should follow PWM input.

4. Finish demodulator and gather data.

   (i) Disconnect DC signal source from PWM input and **reconnect** LSA output.

   (ii) Use function generator on **LSA input** to generate a **SINE WAVE**.
   - Frequency: 2 kHz (or 1 kHz or 5 kHz if results look better)
   - Amplitude: 1 V (i.e., $2\,V_{\text{peak-to-peak}}$) with $0\,V_{DC}$ offset (does offset matter?)

   (iii) Use oscilloscope to view **ramp output**.
   - Channel 1: **LSA OUTPUT** (*not* input)
   - Channel 2: Receiver ramp output (i.e., $C1$ waveform)
   - Use **same vertical scale** (e.g., 2 V/div).
   - **Align BOTH grounds** with lowest visible *grid line* on screen.
   - Set **trigger** `Edge` for channel `1`
     - Adjust **level** or **filtering** (see `Mode`) to stabilize **channel** `1`.
     - Channel `2` MAY MOVE.
   - Choose **HORIZONTAL SCALE** that shows one *full* period (e.g., 50 μs/div).
   - Press `Single` to see relationship between signals.
     - You should see **ramps** that peak at **LSA output** and then **reset** (like PWM/ADC lab).
   - **SAVE A PLOT** and toggle `Run/Stop` back to **green**.

   (iv) Use oscilloscope to view **sample-and-hold output**.
   - Channel 1: **LSA OUTPUT** (*not* input)
   - Channel 2: First sample-and-hold output (i.e., $C2$ waveform)
   - Use **same vertical scale** (e.g., 2 V/div) and **horizontal scale** (e.g., 50 μs/div) as before.
   - **Align BOTH grounds** with lowest visible *grid line* on screen.
   - Set **trigger** `Edge` for channel `1`
     - Adjust **level/filtering** (see `Mode`) to stabilize **channel** `1`. Channel `2` MAY MOVE.
   - Press `Single` to see relationship between signals.
     - The **ramps** from before should now be followed by a **HOLD**.
     - HOLD fills in gap from reset (i.e., holds output while waiting for next receiver pulse).
     - Removing $C2$ does not alter output. Why? (hint: tiny air gap between OA pins 3 & 4)
   - **SAVE A PLOT** and toggle `Run/Stop` back to **green**.

   (v) Use oscilloscope to view **demodulator output**.
   - Channel 1: **LSA OUTPUT** (*not* input)
   - Channel 2: Second sample-and-hold output (i.e., $C3$ waveform)
   - Use **same vertical scale** (e.g., 2 V/div) and **horizontal scale** (e.g., 50 μs/div) as before.
   - **Align BOTH grounds** with lowest visible *grid line* on screen.
   - Set **trigger** `Edge` for channel `1`
     - Adjust **level/filtering** (see `Mode`) to stabilize **channel** `1`. Channel `2` MAY MOVE.
   - Press `Single` to see relationship between signals.
     - You should see a **Sampled-and-Held** version of *delayed* LSA output.
     - NEW hold fills in gap from ramp (i.e., holds output while ramp rises to next value).
   - **SAVE A PLOT**.
     - Why is there distortion? Can it be removed? How?
     - How would 20 kHz LSA output (i.e., from 20 kHz LSA input) compare to demod. output?
     - What would show up on the demodulator output for a 1 Hz LSA ***input***?
     - Why do we reset the ramp generator using a ***delayed*** version of the received IR pulses?