ECE 327: *Electronic Devices and Circuits Laboratory I*

Procedure for Lab 5 (Analog-to-Digital Conversion (ADC) Lab)

SEE LAB *BOOK*. The questions you must answer **in your report** are given in the book.

Bypass capacitors: Unless otherwise noted, **bypass capacitors** terminate at $0\,V_{DC}$.

Construction: **YOU WILL KEEP EVERYTHING** that you build in this laboratory. Build your circuits to be **clean**, **accessible**, and **COMPACT**. **TRY TO BUILD ENTIRE TRANSMITTER IN *SAME* BREADBOARD "*COLUMN*."** Be sure to make the ***LSA input***, ***LSA output***, and ***PWM output*** *EASY TO FIND* in later laboratories; these signals are used often.

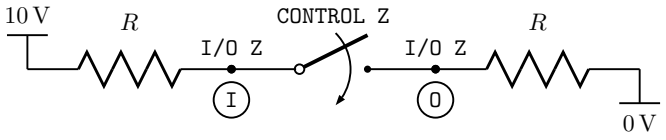
0. **BY NOW**, you should be using a $10\,V_{DC}$ regulated supply for the *transmitter*. If you have not constructed your regulator. See the supplementary text for details. To ensure good performance, pay attention to bypass capacitors. **Everything** you build today will use this **regulated rail**.

1. Design, build, and test the level-shifter amplifier (LSA)

   - See supplementary text for LSA schematics – **Use 10 V and 0 V supply rails**
     - Choose an LSA (the OA LSA is **recommended**) — for tuning, **USE potentiometers!**
       - For the OA LSA, the C_B bypass capacitor and the LM741 OA are **recommended**
       - For the transistor-based LSA, use the "Good LSA" (i.e., attenuate signal first)
     - A **small bypass capacitor** (e.g., $0.1\,\mu$F ceramic) at $10\,V_{DC}$ pin improves *PSRR*
     - **TO PREVENT EXPLOSIONS**, avoid **polarized** (e.g., electrolytic) **capacitors**
       - ⋆ Using **high input *resistances*** allows you the use of smaller coupling capacitors
       - **Alternative**: combine small ceramic capacitors (e.g., use two $1\,\mu$F in parallel for $2\,\mu$F)
       - Make sure cathode (i.e., "negative" end) connected to lower DC voltage
       - **Stand back from circuit** for a few seconds after turning on power
       - **Be prepared** to turn supply off if a capacitor explodes
     - **LSA input** and **LSA output** are frequently used; **MARK THEM FOR EASY ACCESS**
   - Generate a **sine wave** as a test input
     - Input (oscilloscope channel 1 at 2 V/div with ground on second-highest grid line):
       - Frequency: 5 kHz (**after tuning**, try signals from 20 Hz to 15 kHz)
       - Amplitude: 1 V (i.e., $2\,V_{peak\text{-}to\text{-}peak}$) — enable Ampl -20dB on *old* function generators
       - DC offset: $0\,V_{DC}$ (**after tuning**, try **small** offset; **careful** with electrolytic capacitors)
     - **Expected output** (scope channel 2; 2 V/div; ground on lowest grid line): $-3 \times \text{input}_{AC} + 5\,V$
       - Frequency: Same as input (e.g., 5 kHz)
       - Amplitude: 3 V (i.e., $6\,V_{peak\text{-}to\text{-}peak}$, but *inverted* with respect to input)
       - DC offset: $5\,V_{DC}$ (i.e., signal swings from 2–8 V)
       - **No phase shift:** If you see phase shift, your input capacitor and/or resistor are *too small*
     - Setup oscilloscope measurements
       - Use Quick Meas on Source 1 (i.e., **input**) to show Peak to Peak (should be 2 V)
       - Use Quick Meas on Source 2 (i.e., **output**) to show Peak to Peak (should be 6 V)
       - Use Quick Meas on Source 2 (i.e., **output**) to show Average (should be $5\,V_{DC}$)
       - For cleaner measurements, turn on Averaging under Acquire (use **low** # of samples)
       - To reduce output noise, use power supply *bypass capacitors* at regulator, clock, and LSA
     - **Tune gain and offset** until output is correct (again, **use potentiometers!**)
     - **SAVE A PLOT** showing **input**, **output**, and **measurements** on same screen
     - Some **possible** discussion topics for report:
       - How does DC offset of input affect output?
       - How does frequency of input affect output?
       - How does temperature affect performance? Better or worse with op. amp implementation?

2. Design, build, and test pulse-width-modulation (PWM) circuit

- See book's Figure 5.7: Pulse-Width Modulator
  - For **every component**, use 0 V and **regulated** 10 V supply rails
    - **NOTE:** $GND = V_{EE} = V_{SS} = 0\,\text{V}$ and $V_{CC} = V_{DD} = 10\,\text{V}$
  - See supplementary text for **ramp generator** schematics. Use your *true* clock period for "T."
    - Choose one of the two circuit options
    - **USE POTENTIOMETER** for R_1–R_2 divider or R_E resistor
    - Use CD4066 for switch — **TEST SWITCH BEFORE** connecting to circuit
      - **First,** ensure that $V_{SS} = 0\,\text{V}$ and $V_{DD} = 10\,\text{V}$
      - Construct the testing circuit shown below, where $R = 1\,\text{k}\Omega$



CONTROL	⟹	I	O
0 V	⟹	10 V	0 V
10 V	⟹	5 V	5 V

      - For safety, use a 1–1.5 kΩ resistor for `CONTROL` connections (i.e., instead of simple "wire")
      - For 0 V *control*, use DMM to verify switch *input* sees 10 V and switch *output* sees 0 V
      - For 10 V *control*, use DMM to verify *input* **and** *output* ***BOTH*** see ***the same*** 5 V
      - **TEMPORARILY** connect control to 30 kHz clock and verify **no switch delay**
      - Repeat until **ONE** working switch is found — only get a new chip if **ALL** switches fail
      - **DISCONNECT switch testing circuit** (but leave V_{SS} and V_{DD} connected)
    - Calculate desired $i_C = C\,\text{d}v_C/\text{d}t$ for appropriate ramp slope (ramp slope is $\text{d}v_C/\text{d}t$)
      - Pick slope so that $(8\,\text{V})/(T - 6\,\mu\text{s}) \le \text{d}v_C/\text{d}t \le .333\,\text{V}/\mu\text{s}$ for your *true* clock period T
      - Start with $C = 2.2\,\text{nF}$ (code: `2n2` or `222`) — in most cases, this value is a good choice
    - Pick biasing circuit and R_E to to implement i_C source
      - Make biasing circuit, R_E, or both **TUNABLE**
    - To **TEST** your ramp generator, **temporarily** connect its *Reset* input (i.e., the FET control) to a 30 kHz 0–10 V clock (e.g., **from your 555 circuit** or a function generator)
      - The ramp generator output should be a train of **ramps and resets**
      - If ramps are **noticeably round** and resets **vertical**, try *reconfiguring* for a *higher* C
      - If ramps are **linear** and resets **very curved**, try *reconfiguring* for a *lower* C
      - **DO NOT TUNE your ramp *slope* at this time**
      - **DISCONNECT** *Reset* from clock when done testing
      - *Reset* will eventually be tied to $\overline{Q}$ on your JK flip–flop
    - *OPTIONAL*: Use **small (ceramic) bypass capacitor** at supply pin (i.e., $10\,\text{V}_{\text{DC}}$ input)
  - Use LM311 voltage comparator with *open-collector* output
    - CAUTION: Pin-out *similar* to op. amp., but *inputs are swapped*
    - **CAUTION**: There is a **GROUND** pin **AND** a **V-**. Connect them **BOTH** to 0 V.
    - Output **must be pulled-up** to $10\,\text{V}_{\text{DC}}$ **with a 1 kΩ resistor** (code: brown-black-red)
      - *OPTIONAL*: Use **small (ceramic) bypass capacitor** at resistor's $10\,\text{V}_{\text{DC}}$ supply pin
    - Non-inverting input (i.e., "+" input) tied to **ramp generator output's** capacitor voltage
    - Inverting input (i.e., "−" input) is **PWM input**, so **MARK IT FOR EASY ACCESS**
    - **DO NOT** connect the **LSA output** to the **PWM input**
      - You're not ready for that YET

  - Use a JK flip–flop from CD4027 (or D-type CD4013; pin-out: swap J & K pins for D pin)
    * Connect power rails so that $V_{DD} = 10\,\text{V}$ and $V_{SS} = 0\,\text{V}$
    * Configure so output Q goes *high* **on clock edge:**
      · CLK tied to 30 kHz clock from previous lab (i.e., pin 3 of 555)
      · J (or D) tied to 10 V (i.e., *high*)
      · K tied to 0 V (i.e., *low*)
    * Configure so output goes *low* **asynchronously** by comparator output:
      · S tied to 0 V (i.e., *low*)
      · R tied to comparator output
    * Configure so ramp generator is reset when output is *low*:
      · $\overline{Q}$ tied to ramp's "reset" input (i.e., the CD4066 switch control)
      ⋆ For safety, use a 1.5 kΩ resistor (code: brown-green-red) to make this connection
    * *OPTIONAL*: Use **small (ceramic) bypass capacitor** at V_{DD} pin (i.e., 10 V_{DC} input)
    * Output Q is **PWM output**, so **MARK IT FOR EASY ACCESS**
- Test and tune PWM circuit
  - **Apply** 2 V_{DC} to 8 V_{DC} to **PWM input** (i.e., comparator's "−" input)
    * Generate with second DC supply output **OR** the *wiper* of a potentiometer between rails
  - Connect oscilloscope to circuit
    * Channel 1: Capacitor waveform (i.e., **ramp output**) at 2 V/div
    * Channel 2: **PWM output** at 10 V/div
    * Set oscilliscope **trigger** `Edge` for **RISING** transitions on source `2`
    * **Separate** channels: put ramp ground on lowest grid line and PWM ground on 2nd highest
  - Use `Quick Meas` to measure: `Maximum` of `1`, and `+ Width` and `− Width` of `2`
  - Manually vary **DC input** slowly (i.e., oscillate from 2 V to 8 V) and observe:
    (i) Slope of ramp
    (ii) Maximum height of ramp (compared to input)
    (iii) Relationship (in time) between ramp and PWM output
    (iv) `+ Width` (i.e., time per period that output is ***high***)
    (v) `− Width` (i.e., time per period that output is ***low***)
  - **TUNE** ***ramp generator current*** **(i.e., ramp slope) until ALL of the following:**
    (i) *IMPORTANT:* The sum of `+ Width` and `− Width` is *equal* to your **clock period**
      * If it is too *large,* then *greatly increase slope* until compliant
    (ii) `+ Width` for constant 2 V_{DC} PWM input is 6 μs or greater
    (iii) `− Width` for constant 8 V_{DC} PWM input is 6 μs or greater
  - **AFTER TUNING**, show **ramp output** and **PWM output** at both extremes
    * Use `Quick Meas` to show `+ Width`, output `− Width`, and ramp `Maximum`
    * For 2 V_{DC} input, **SAVE A PLOT** showing **PWM**, **ramp**, and **measurements**
    * For 8 V_{DC} input, **SAVE A PLOT** showing **PWM**, **ramp**, and **measurements**
  - Using `Cursors`, **DETERMINE THE SLOPE** (in V/μs units) of the ramp output
    * **MAKE SURE** that cursor `Source` is set to your **ramp channel (i.e., `1`)!!!!**
    * **SAVE A PLOT** showing **ramp** and `Cursors` with slope information (i.e., ΔX, ΔY)
- Some **possible** discussion topics for report:
  - What is the relationship between input and ramp output? . . . ramp output and PWM output?
  - What determines the slope of the falling edge of the ramp? Why is it not totally vertical?
  - Why are 2 V_{DC} and 8 V_{DC} important inputs?
  - How does temperature affect performance? (hint: consider ramp generator's current source)
    * An LM317 can be used as a current source — assuming DO ≈ 1 V, why can't we use it?

3. Connect LSA to PWM
   - *Disconnect* 2–8 V_{DC} input from **PWM input** (i.e., comparator's "−" input)
   - Connect **LSA output** (i.e., op. amp. output) to **PWM input** (i.e., comparator's "−" input)
   - Generate a **sine wave** as a test input **to LSA**
     - LSA Input:
       * Frequency: 5 kHz
       * Amplitude: 1 V (i.e., 2 $V_{peak\text{-}to\text{-}peak}$) — enable [Ampl -20dB] on *old* function generators
       * DC offset: 0 V_{DC}
   - View *LSA output* and *ramp generator output*
     - Channel 1: **LSA OUTPUT** at 2 V/div
     - Channel 2: **ramp generator output** at 2 V/div
     - **ALIGN both channel grounds** on lowest grid line
     - Set oscilliscope **trigger** [Edge] for source [1]
       * Adjust **trigger level knob** or **trigger filtering** (see [Mode]) until **channel** [1] stabilizes
       * The input and output are naturally **asynchronous**, so channel [2] MAY MOVE
     - Note the relationship between the two channels. TRY VARIOUS **horizontal (time) scales**
     - Press [Run/Stop] or [Single] to pause display
     - **[SAVE A PLOT]** and **THEN** toggle [Run/Stop] back to **green**
   - View *ramp generator output* and *PWM output*
     - Channel 1: **ramp generator output** at 2 V/div
     - Channel 2: **PWM output** at 10 V/div
     - Set oscilliscope **trigger** [Edge] for **RISING** transitions on source [2]
     - **Separate** channels: put ramp ground on lowest grid line and PWM ground on 2nd highest
     - Press [Single]. Note the relationship between the two channels
     - **[SAVE A PLOT]** and THEN toggle [Run/Stop] back to **green**
   - View *LSA **INPUT*** (*NOT* output!) and *PWM output*
     - Channel 1: **LSA INPUT** (*NOT* output!) at 2 V/div
     - Channel 2: **PWM output** at 5 V/div
     - Set oscilliscope **trigger** [Edge] for source [1]
       * Stabilize **channel** [1] ([2] can move) with **level knob** or **filtering** (see [Mode])
     - **Separate** channels on the screen
     - Press [Single]. Note the relationship between the two channels
     - **[SAVE A PLOT]**
   - Some **possible** discussion topics for report:
     - What are the relationships among the LSA input, ramp output, and PWM output?
       * Given an input signal, how can the other signals be predicted?
       * What is the relationship between input amplitude and output pulse width?
     - Given that a walkman output has a 15 kHz bandwidth, what is the rationale for using a 30 kHz carrier in the PWM circuit?
     - How does temperature affect performance? (hint: how does the ramp generator work?)
     - Why (and how) does the C value change the *curviness* of the "sawtooth" characteristics?
     - The output of this circuit can be viewed as a string of 0's and 1's (i.e., it takes 2 states). However, it is not an ADC. Why not? (hint: can you *count* the number of "adjacent" 1's?)
     - The PWM circuit could be called an ADC if the positive width of each pulse was counted (e.g., in terms of high-speed clock cycles). What would set the *resolution* of such an ADC?