Dual-Rail Level-Shifter Amplifiers

Lab 5: Analog-to-Digital Conversion

ECE 327: *Electronic Devices and Circuits Laboratory I*

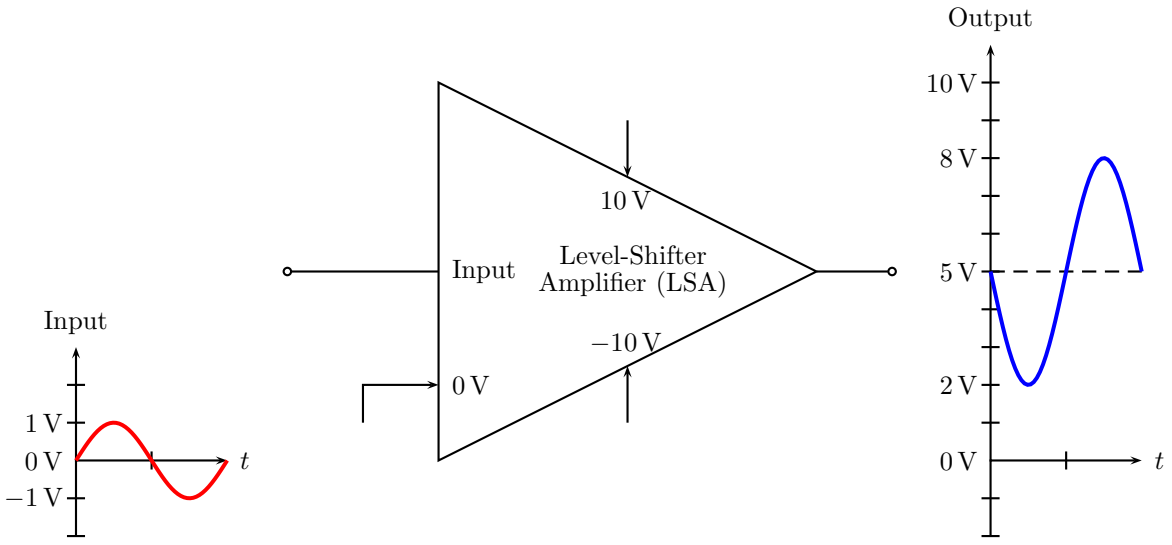
Abstract

For the analog-to-digital conversion lab (and others), we need to implement a single-rail (i.e., 10 V and 0 V "rails") level-shifter amplifier (LSA). In this document, we explore two dual-rail (i.e., ±10 V rails) LSA approaches. These designs should not be used for the laboratory, as they require a −10 V rail; they are presented here as examples.

Contents

1 Introduction

Our goal is to build a circuit that takes a 2 V peak-to-peak signal centered at 0 V as input and translates it to a 6 V peak-to-peak signal centered at 5 V on its output. That is, we want a component like



The signals available to us are ±10 V and 0 V. The input signal exists within a −1–1 V envelope. The output signal must be a (possibly inverted) version of the input signal that exists within a 2–8 V envelope. Therefore, the *magnitude* of the amplifier gain should be 3 and the amount of DC shift should be 5 V.

Here, we investigate two different methods of implementing the level-shifter amplifier (LSA). The first uses an operational amplifier (OA). The second, a so-called common emitter amplifier, uses an NPN transistor. Lab part pin-outs are given in Appendix A.

2 Operational Amplifier LSA

Consider the OA configuration in Figure 2.1[1].

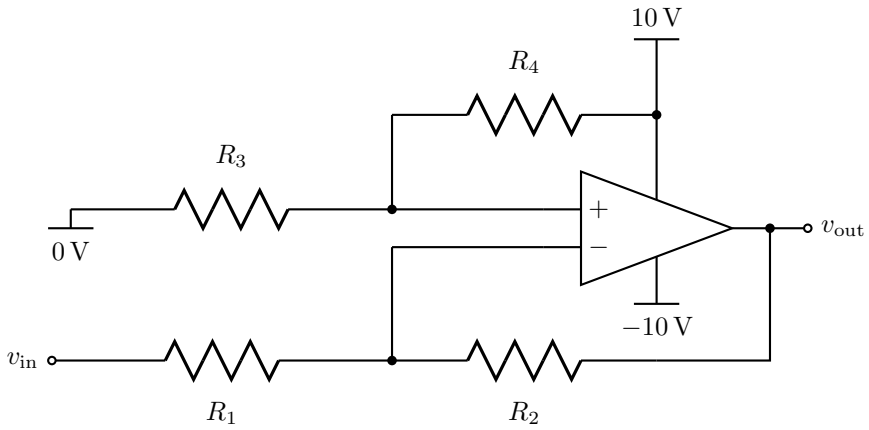


Figure 2.1: Level-shifter amplifier implemented with operational amplifier.

This configuration is nearly identical to an inverting amplifier, but the non-inverting input, which usually has a copy of the ground reference, has been shifted up toward 10 V through a resistive divider. So the (AC) gain of this circuit is still $-R_2/R_1$, but there will be some DC offset set by the values of all four resistors.

The potential at the non-inverting input, v_+, is given by

$$v_+ = (10\,\text{V})\frac{R_3}{R_3 + R_4},$$

and the output potential is given by

$$\begin{aligned} v_{\text{out}} &= v_+ - (v_{\text{in}} - v_+)\frac{R_2}{R_1} \\ &= v_+ - v_{\text{in}}\frac{R_2}{R_1} - v_+\frac{R_2}{R_1} \\ &= v_+\left(1 + \frac{R_2}{R_1}\right) - v_{\text{in}}\frac{R_2}{R_1} \\ &= \underbrace{(10\,\text{V})\frac{R_3}{R_3 + R_4}\left(1 + \frac{R_2}{R_1}\right)}_{\text{DC offset}} - v_{\text{in}}\underbrace{\frac{R_2}{R_1}}_{|\text{Gain}|}. \end{aligned}$$

We know that the gain magnitude should be 3, so

$$\frac{R_2}{R_1} = 3 \tag{2.1}$$

as expected. Therefore,

$$v_{\text{out}} = (1+3)(10\,\text{V})\frac{R_3}{R_3 + R_4} - 3v_{\text{in}} = \underbrace{(40\,\text{V})\frac{R_3}{R_3 + R_4}}_{\text{DC offset}} - 3v_{\text{in}}.$$

We know that the DC offset should be 5 V, so

$$\frac{R_3}{R_3 + R_4} = \frac{5}{40} = \frac{1}{8} = 0.125, \tag{2.2}$$

so $v_+ = 1.25\,\text{V}$. Consider implementing Equation (2.2) with a potentiometer so that v_+ can be tuned.

[1] Ideally, the −10 V rail could be replaced with a 0 V reference to make this design single-ended. Unfortunately, our laboratory OAs will require a slightly negative lower rail.

3 NPN Common-Emitter LSA

Both NPN[2] and PNP[3] common-emitter amplifiers are LSAs by their nature. Here, we focus on the NPN case. However, the same approach could be applied to designing a PNP common-emitter LSA.

First, we introduce the design method using a *single-ended* LSA (i.e., power rails are 10 V and 0 V). We will show that this approach fails to produce an adequate LSA for signals of interest to us. That is, our input signals have too large of a swing to be used with a single-ended LSA being powered by a single 10 V rail. To fix this problem, we could attenuate our input signals and increase our common emitter gain. Unfortunately, increasing amplifier gain also increases output noise. So we show how adding a −10 V rail allows for additional input swing.

Bad LSA: The single-ended case

Consider Figure 3.1. The input is the sum of a DC (i.e., average) part V_{in} and a purely AC (i.e., zero average)

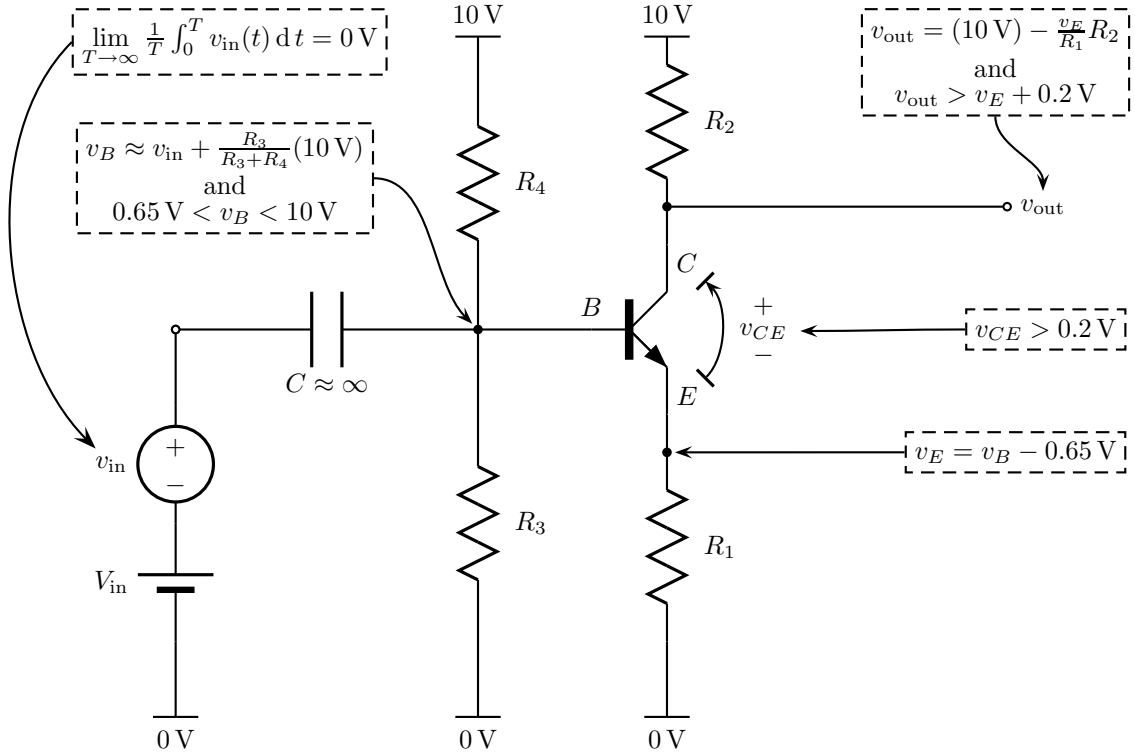


Figure 3.1: Level-shifter amplifier implemented with single-ended common-emitter NPN configuration.

part v_{out}. The capacitor C is meant to AC couple the signal to the base of the transistor. That is, it should be chosen so large that it is a short-circuit to all frequencies of interest. We give guidelines for choosing C later.

First, we pick the values of R_1, R_2, R_3, and R_4 to give us a v_{in} gain magnitude of 3 and DC offset of

[2] "**N**ot **P**ointing i**N**"
[3] "**P**oints i**N** **P**roudly"

5 V. The value of v_{out} is

$$\begin{aligned} v_{\text{out}} &= (10\,\text{V}) - (v_B - 0.65\,\text{V})\,\frac{R_2}{R_1} \\ &= \underbrace{(10\,\text{V}) + (0.65\,\text{V})\,\frac{R_2}{R_1} - \frac{R_2}{R_1}\,\frac{R_3}{R_3+R_4}\,(10\,\text{V})}_{\text{DC offset}} - \underbrace{\frac{R_2}{R_1}}_{|\text{Gain}|}\,v_{\text{in}}. \end{aligned}$$

Because the gain magnitude should be set to 3,

$$\frac{R_2}{R_1} = 3. \tag{3.1}$$

Therefore,

$$v_{\text{out}} = \underbrace{(11.95\,\text{V}) - \frac{R_3}{R_3+R_4}\,(30\,\text{V})}_{\text{DC offset}} - 3v_{\text{in}}.$$

Because the DC offset should be 5 V,

$$\frac{R_3}{R_3+R_4} = \frac{6.95}{30} = \frac{139}{600} = 0.23166\cdots, \tag{3.2}$$

so the transistor base sees a DC average of ∼2.316 V. You could implement Equation (3.2) with a potentiometer so that ouptut offset could be tuned.

Problem: Clipping caused by saturation

It is good practice to make sure that our input signal will not drive our LSA to distort the output. That is, we should make sure the LSA is in compliance at all times for all possible v_{in}.

From Equation (3.2),

$$v_B = v_{\text{in}} + \frac{69.5}{30}\,\text{V} = v_{\text{in}} + 2.3166\cdots\,\text{V}.$$

The input v_{in} ranges from −1 V to 1 V, so

$$1.3166\cdots\,\text{V} < v_B < 3.3166\cdots\,\text{V}.$$

Because $0.65\,\text{V} < v_B < 10\,\text{V}$ at all times, the transistor should always be biased on. Therefore, we should not expect any hard clipping. However, we must make sure the transistor never goes into saturation and distorts the output signal. That is, we must make sure $v_{CE} > 0.2\,\text{V}$ at all times. The emitter potential v_E

$$0.66\cdots\,\text{V} < v_E < 2.66\cdots\,\text{V},$$

and, for the same range, the output v_{out}

$$8\,\text{V} > v_{\text{out}} > 2\,\text{V}.$$

Unfortunately, when the input rises to 1 V, the emitter rises to 2.66 V and the collector (i.e., the output) falls to 2 V. That is, the collector and emitter intersect. As $v_{CE} > 0.2\,\text{V}$ to prevent saturation, the emitter and collector can never intersect. Therefore, the output will be distorted, and so **this LSA should not be used.**

Solution: Input attenuation

Because the NPN transistor saturates, the LSA cannot be used in its present form. However, the input signal can be attenuated so that the emitter swing is less than 1.8 V. Of course, the R_2/R_1 gain will need to increase by the same factor to maintain the 6 V output swing. For example, if the input to the common emitter amplifier has a 1 V swing and $R_2/R_1 = 6$, the output will have the desired characteristics.

Attenuating the input signal must be done with care. If a simple resistive divider is added before the coupling capacitor, the equivalent impedance looking into the capacitor must be large. Otherwise, a buffer (e.g., a voltage follower) must be used. Additionally, because the gain of the common emitter amplifier has been increased, a larger noise component will show up on the output. Thus, it may be impractical to implement the LSA this way.

Good LSA: Using both rails for extra swing

Consider Figure 3.2, which is identical to Figure 3.1 except that 0 V is only used to reference the input (and output); −10 V is used as a reference for the rest of the circuit.

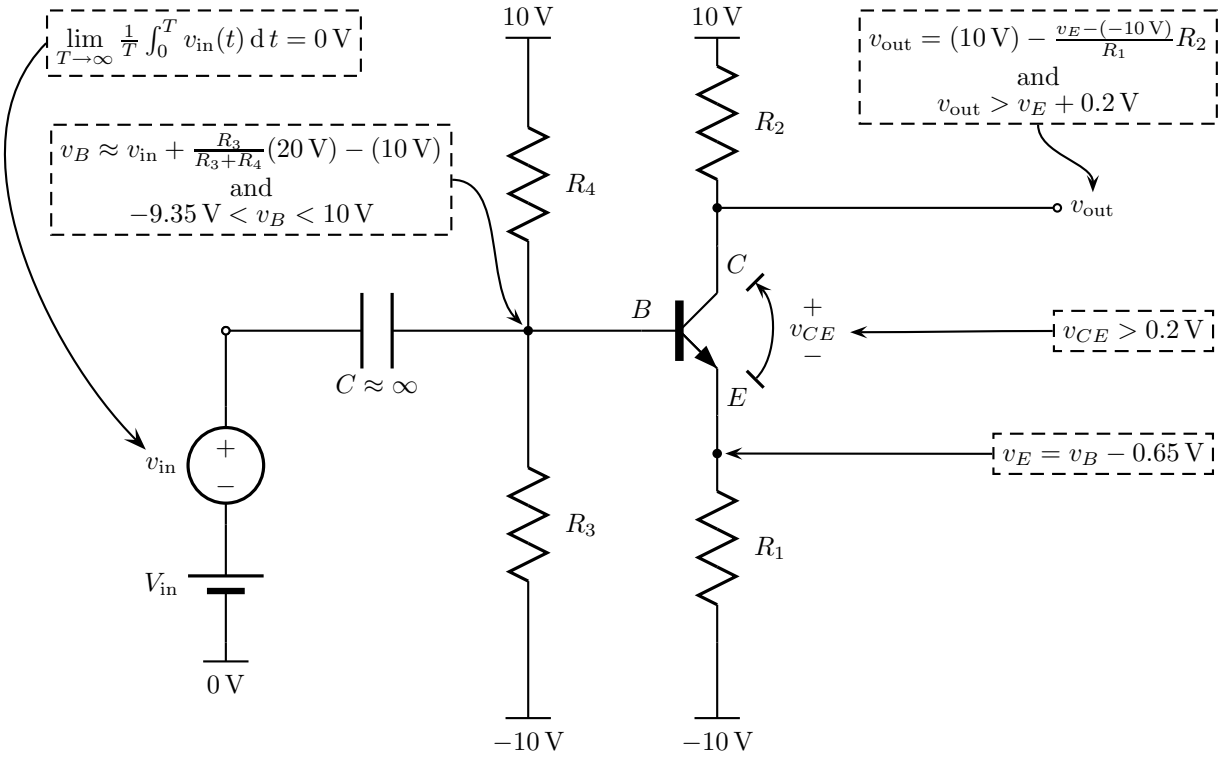


Figure 3.2: Level-shifter amplifier implemented with dual-rail common-emitter NPN configuration.

Using the −10 V rail this way changes very little. The most significant operational difference is that v_{CE} is much larger during operation. Transistors may be viewed as flexible resistors that stretch to displace other elements in a circuit. In this case, v_{CE} is holding the downward swinging output of the circuit away from the upward swinging input of the circuit. The NPN transistor we use in the lab, a 2N3904, has a v_{CE} breakdown of 40 V, so we should safely be able to use this transistor in our application[4].

Again, we need to pick the values of R_1, R_2, R_3, and R_4 to give us v_{in} gain magnitude of 3 and DC offset of 5 V. The value of v_{out} is

$$\begin{aligned} v_{\text{out}} &= (10\,\text{V}) - (v_B - (0.65\,\text{V}) + (10\,\text{V}))\,\frac{R_2}{R_1} \\ &= (10\,\text{V}) - \left(v_{\text{in}} + \frac{R_3}{R_3+R_4}(20\,\text{V}) - (10\,\text{V}) - (0.65\,\text{V}) + (10\,\text{V})\right)\frac{R_2}{R_1} \\ &= \underbrace{(10\,\text{V}) + (0.65\,\text{V})\,\frac{R_2}{R_1} - \frac{R_2}{R_1}\frac{R_3}{R_3+R_4}(20\,\text{V})}_{\text{DC offset}} - \underbrace{\frac{R_2}{R_1}}_{|\text{Gain}|}\,v_{\text{in}}. \end{aligned}$$

Because the gain magnitude should be set to 3,

$$\frac{R_2}{R_1} = 3. \tag{3.3}$$

[4]However, we will dissipate more power through the transistor, as expected by the power–distortion tradeoff. Additionally, thermal runaway may reduce the base-emitter drop required for excitation, and so our signal may drift toward saturation.

Therefore,

$$v_{\text{out}} = \underbrace{(11.95\,\text{V}) - \frac{R_3}{R_3 + R_4}\,(60\,\text{V})}_{\text{DC offset}} - 3v_{\text{in}}.$$

Because the DC offset should be 5 V,

$$\frac{R_3}{R_3 + R_4} = \frac{6.95}{60} = \frac{139}{1200} = 0.115833\cdots. \tag{3.4}$$

The divider in Equation (3.4) yields half the the ratio of Equation (3.2). The current through R_3 has been doubled by using the -10 V as a reference; however, for proper biasing, the drop across the R_3 resistor has remained the same. Therefore, R_3's contribution to the R_3–R_4 divider has been halved. The base of the transistor sees a DC average of approximately -7.683 V, which is 2.317 V above the -10 V rail. You should consider implementing Equation (3.4) with a potentiometer so that the output offset can be tuned.

Compliance and linearity

It is good practice to make sure that our input signal will not drive our LSA to distort the output. That is, we should make sure the LSA is in compliance at all times for all possible v_{in}.

From Equation (3.4),

$$v_B = v_{\text{in}} + \left(\frac{130}{60}\,\text{V}\right) - (10\,\text{V}) = v_{\text{in}} - 7.6833\cdots\,\text{V}.$$

The input v_{in} ranges from -1 V to 1 V, so

$$-8.6833\cdots\,\text{V} < v_B < -6.6833\cdots\,\text{V}.$$

Because $-9.35\,\text{V} < v_B < 10\,\text{V}$ at all times, the transistor should always be biased on. Therefore, we should not expect any hard clipping. However, we must make sure the transistor never goes into saturation and distorts the output signal. That is, we must make sure $v_{CE} > 0.2$ V at all times. For emitter potential v_E,

$$-9.33\cdots\,\text{V} < v_E < -7.33\cdots\,\text{V},$$

and, for the same range, the output v_{out} is such that

$$8\,\text{V} > v_{\text{out}} > 2\,\text{V}.$$

When the input rises to 1 V, the emitter rises to $-7.33\cdots$ V and the collector (i.e., the output) falls to 2 V. Here, the emitter and collector are far away from the v_{CE} saturation limit of 0.2 V. Therefore, not only is this LSA adequate (i.e., it is always in compliance), but we should expect its performance to be very linear (i.e., the signal should have minimal distortion).

Choosing a coupling capacitor

Next, we give some guidelines for choosing a sufficiently large C. Capacitor C and the parallel combination $R_3 \| R_4$ form an RC high-pass filter between the input and the transistor base. The filter has the transfer function

$$\frac{R_3 \| R_4}{\frac{1}{sC} + R_3 \| R_4}, \quad \text{which is} \quad \frac{1}{\frac{1}{s(R_3 \| R_4)C} + 1}.$$

Let f be the half power (i.e., -3 dB) corner frequency of this filter. Then, the capacitance C is

$$C = \frac{1}{2\pi f (R_3 \| R_4)},$$

and so

$$R_4 C = \frac{1}{2\pi f}\frac{1}{\frac{R_3}{R_3+R_4}} = \frac{1}{\pi f}\frac{600}{139} \approx \frac{1.374}{f}.$$

We would like f to be as low as possible. We could tune both R_4 and C to be very large; however, it's better to keep R_3 and R_4 small (e.g., $R_3 \| R_4 \ll \beta R_1$, where $\beta \approx 100$, so R_3 and R_4 might be in the neighborhood of 1–10 kΩ). Therefore, make C very large, so that

$$C \geq \frac{1.374}{f R_4} = 69\,\mu\text{F}, \tag{3.5}$$

where $f \approx 20$ Hz, the lowest frequency most humans can hear[5], and $R_4 \geq 1\,\text{k}\Omega$[6].

Capacitors of this high magnitude[7] are usually polarized (e.g., tantalum or electrolytic capacitors). In a real design, capacitor dielectric is chosen to provide the least distortion for signals of interest. In *our laboratory*, only electrolytic capacitors are available. **Make sure your polarity is set correctly. Otherwise, your capacitor may *explode*.** Because $V_{\text{in}} = 0$ V and the base DC bias point is *negative*, the input should connect to the *positive* end of the capacitor[8], as shown in Figure 3.3 and Figure 3.4.

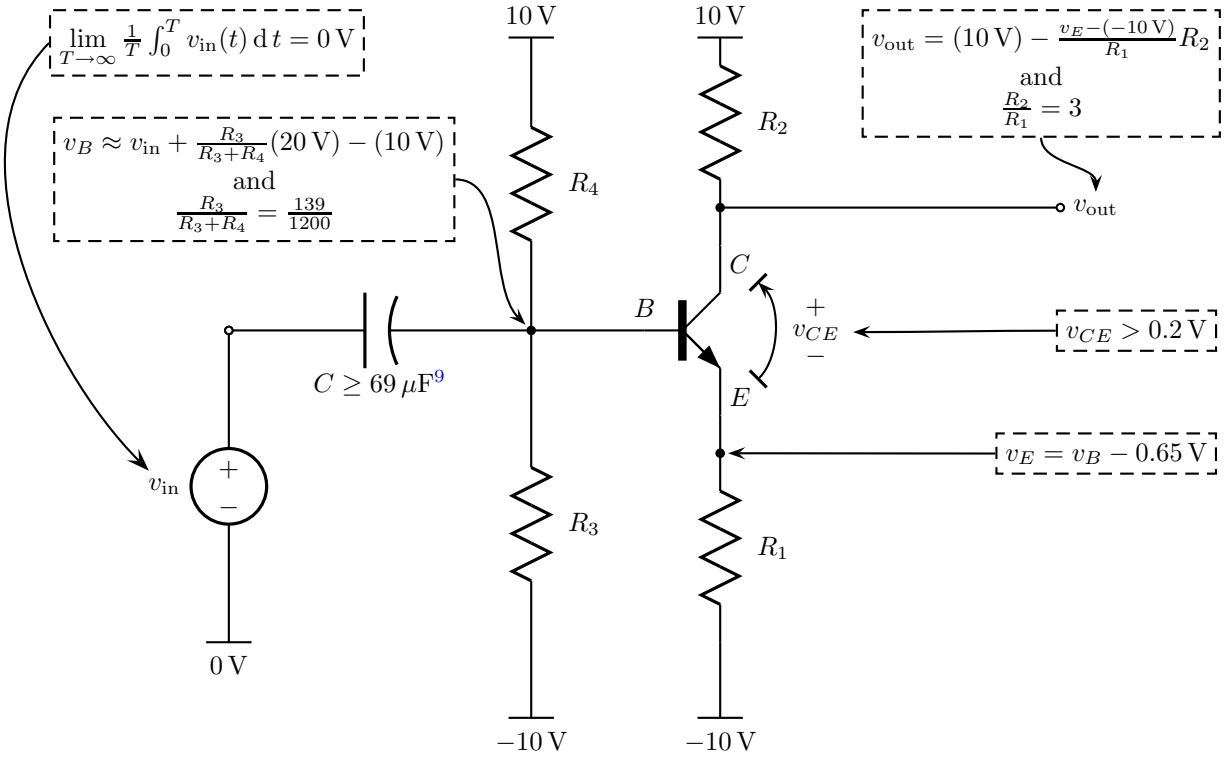


Figure 3.3: Dual-rail common-emitter NPN LSA with component values shown.

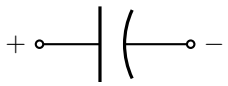


Figure 3.4: Chemical (e.g., electrolytic) capacitor symbol convention.

[5] Our input should never have frequencies this low, so this bound is ultra conservative.
[6] A 5 kΩ bound might be more realistic.
[7] A much more practical lower bound is 1 μF.
[8] Again, a smaller (e.g., 4.7 μF) capacitor is probably a better choice.
[9] It is more practical to choose a capacitor no larger than 4.7 μF.

Improving linearity and simplifying

The linearity of this LSA is already very good. However, if better linearity is needed, an operational amplifier can be used to adjust the base current dynamically to maintain the appropriate collector current at all times. Consider Figure 3.5.

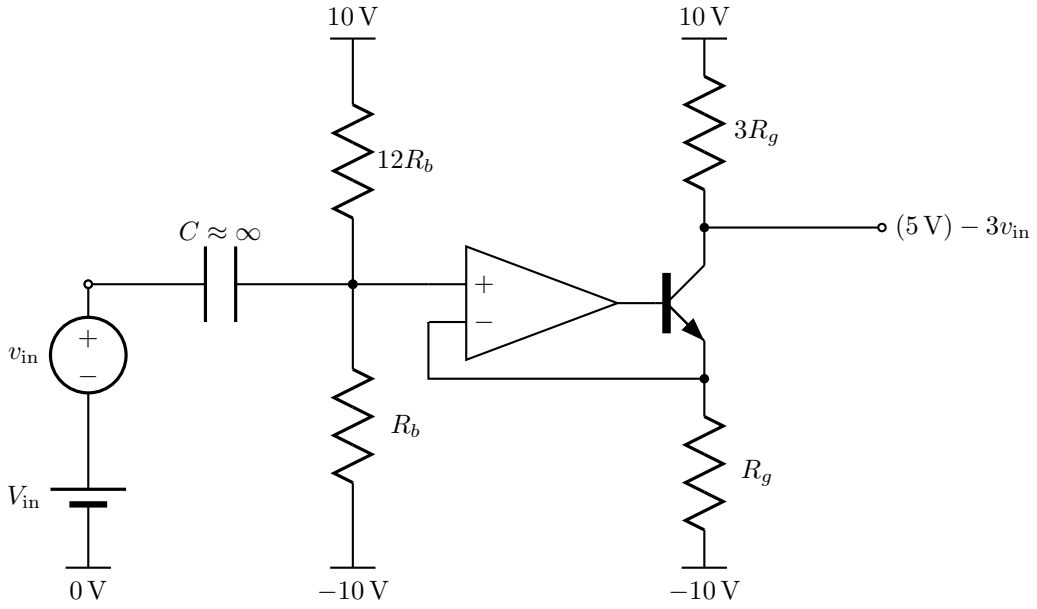


Figure 3.5: Improving NPN transistor linearity with operational amplifier feedback.

Analysis of the new design:

OA input: When the input is turned off (i.e., $v_{\mathrm{in}} \equiv 0\,\mathrm{V}$), the R_b divider places $(5/3)\,\mathrm{V}$ at the noninverting input of the OA.

OA output: The OA adjusts the base current into the transistor so that the emitter also sees $(5/3)\,\mathrm{V}$. Because the OA finds this base current via feedback, we do not need to consider the $0.65\,\mathrm{V}$ base-emitter diode drop in the design. In fact, the OA feedback reduces our design's sensitivity to base-emitter variations (e.g., temperature and manufacturing).

Circuit output: The emitter current matches the collector current, and so there is a gain of 3. However, because the quiescent emitter potential is $(5/3)\,\mathrm{V}$, the output is shifted up by $5\,\mathrm{V}$, as desired.

This circuit performs very well, and its design is straightforward. The buffering effect (i.e., low output impedance and high input impedance) of the OA allows R_g and R_b to be chosen independently of each other, and so it's safe to choose a large R_b and a small R_g. For low-frequency half-power input frequency f, the coupling capacitor C is such that

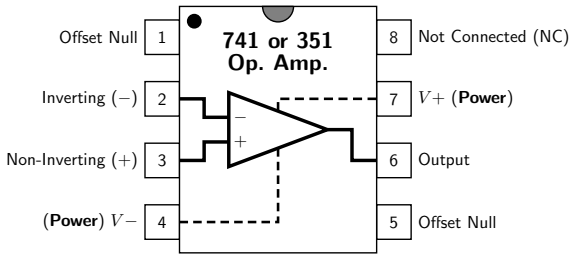
$$C = \frac{1}{2\pi f(R_b \| 12R_b)} = \frac{13}{24\pi f R_b}.$$

Choosing a large R_b lets us pick a small coupling capacitor C. That is, because we now can pick a large R_b independent of the choice of R_g, we can use a small C without having to choose a very large R_g[10].

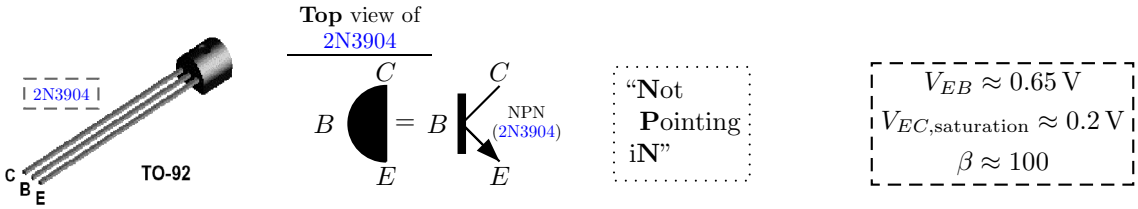
OA choice: The output of the operational amplifier only needs to swing as far and as fast as the input signal. Additionally, in this configuration its output does not need to source much current. Therefore, an LM741 may be appropriate for this use. If additional speed is needed, use an LF351.

[10] Large output resistors can reduce circuit speed for some loads.

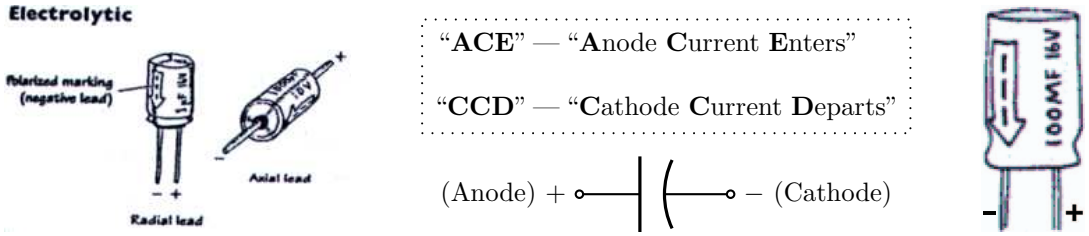
A Parts



(a) LM741/LF351 operational amplifier



(b) 2N3904 NPN BJT transistor



(c) Electrolytic capacitor

Figure A.1: Part pin-outs.