ECE 327: *Electronic Devices and Circuits Laboratory I*

Procedure for Lab 4 (Oscillators Lab)

SEE LAB *BOOK* procedure for information on what you need for your **lab report**.

1. In your book, see Figure 4.3: Op-Amp Relaxation Oscillator
   - Build 1 kHz oscillator with LM741 (use ± 5 V supply rails)
     - Set **period** $T = 2RC\ln(3)$ for 1 kHz frequency (note: nano = 10^{-9}, pico = 10^{-12})
       - Keep $C \geq 100$ pF to dominate parasitic capacitances and $R \geq 1\,\text{k}\Omega$ to reduce power draw
     - View **output** and **capacitor** waveforms on same screen
       - **ALIGN grounds** and use 2 **V/div on both channels**
     - Use `Quick Meas` to determine `Period`, `Frequency`, and `Peak-to-Peak` of **output**
       - Does the LM741 look like a "rail-to-rail" operational amplifier?
     - **SAVE A PLOT** showing **OUTPUT** and **CAPACITOR** waveforms and measurements
   - Adjust *time scale* (i.e., time per division) to "zoom in" to see the *slope* of an an output "edge"
     - Use `Cursors` to find slope of LINEAR PORTION of the "edge"
     - **Give slope in** V/μ**s units** and compare to expected (what is **expected** for an LM741?)
     - **SAVE A PLOT** showing sloped edge and ΔX and ΔY from cursors (no capacitor)
     - **HOW** does the finite slope limit the fastest realizable frequency? Can RC be *too* small?
       - Decrease RC *substantially* to show how the *apparent shape* of the "square" wave changes
       - **SAVE A PLOT** of "trapezoidal" waveform. Show cursors' ΔX and ΔY of edge slope
       - Note that the *edge slope* is **NOT** changing. What is happening? What if $RC \approx 0$?
   - Replace LM741 with LF351 (does the LF351 look like a "rail-to-rail" operational amplifier?)
     - "Trapezoid" sides should have steeper slope ("zoom-in" more if necessary)
     - Use `Cursors` to find slope of LINEAR PORTION one "side" of "trapezoid"
     - **Give slope in** V/μ**s units** and compare to expected (what is **expected** for an LF351?)
     - **SAVE A PLOT** showing sloped edge and ΔX and ΔY from cursors (no capacitor)

2. In your book, see Figure 4.9: Monostable 555 Circuit
   - Set **output pulse width** $T = RC\ln(3)$ to 100 μs
     - Keep $C \geq 100$ pF to dominate parasitic capacitances and $R \geq 1\,\text{k}\Omega$ to reduce power draw
   - Use 0 V and 10 V **supply rails**; use 2.2 nF (code: `2n2` or `222`) *control* capacitor on pin 5 of 555
   - Trigger with 0–10 V square wave with **LOW *pulse width*** between 50–100 μs
     - Frequency: 5–10 kHz (**NO** higher or lower!)
     - 5 V **amplitude** with 5 V **OFFSET—TRIGGER MUST NOT GO NEGATIVE!**
       - Use oscilloscope to **VERIFY** 0–10 V trigger
       - **ON OLD FUNCTION GENERATORS**, you may need to use ~2.5 V offset
     - Use scope trigger `Edge` configuration to synchronize with 555 trigger
       - Select **soft button** to trigger off of **input** (i.e., function generator) channel
       - Select **soft button** to trigger on **downward-going edges**
     - Use `Cursors` to determine **pulse width** of 555 **output**
       - ALTERNATIVELY, use `Quick Meas` on your **output** channel to measure `+ Width`
         - If measurement is jumpy, enable `Averaging` under `Acquire` with 1 `#` of samples
       - **SAVE A PLOT** of the **TRIGGER INPUT** and **555 OUTPUT** on same screen
   - To make trigger pulse greater than 100 μs, **decrease frequency** below 5 kHz
     - **SAVE A PLOT** of misbehaving results—what happens when trigger is **low** for too long?
     - **IN REPORT**, use operation of SR latch to explain results ($S = R = 1$?)

3. In your book, see Figure 4.8: Astable 555 Circuit — **KEEP OSCILLATOR** for quarter project
   - Assemble in **small area near edge** of breadboard (e.g., in *corner* near LM317 regulator circuit)
   - Somehow **MARK CLOCK OUTPUT** so you can find it later
   - Use 0 V and 10 V supply rails
     - Consider using 0.1–2 μF *bypass capacitor* at V_{CC} pin
       - What is the impact of periodic capacitor charging current on rails? Inductance?
       - What is the impact of capacitor discharging on "steadiness" of nearby ground references? What happens to metal when current flows through it?
       - Why do designers use separate power planes for analog and digital components?
       - When analog and digital planes must match, why are they often connected with *inductors*?
   - Use 2.2 nF (code: `2n2` or `222`) *control* capacitor on pin 5 of 555
   - Choose R_A and R_B to **set *duty cycle* Δ (given in %) equal to 60%**, where

     $$\Delta = 100\% \times \frac{R_A + R_B}{R_A + 2R_B}$$

     To find R_A and R_B, it may be easier to use

     $$\frac{R_A}{R_B} = \frac{2\Delta - 100\%}{100\% - \Delta} \quad \text{or} \quad \frac{R_A}{R_A + R_B} = 2 - \frac{100\%}{\Delta} \quad \text{or} \quad \frac{R_B}{R_A + R_B} = \frac{100\%}{\Delta} - 1$$

     where $\Delta \approx 60\%$
   - Set **period** $T = (R_A + 2R_B)C\ln(2)$ for 30 kHz frequency
     - Keep $C \geq 100$ pF to dominate parasitic capacitances
     - Keep $R_B \geq 1\,\text{k}\Omega$ to reduce power draw
   - Probe **output** and **capacitor** waveforms: set **both** channels for 2 V/div and **ALIGN** grounds
     - Use `Quick Meas` to show `Frequency` and `Duty Cycle` of **output**
     - At this point, **DO NOT TUNE**; explain differences in your report
     - **SAVE A PLOT** with **output** waveform, **capacitor** waveform, and **measurements**
   - BEFORE LEAVING, **oscillator must be TUNED for quarter project** (i.e., not for report)
     - (i) **First**, make sure 10 V supply rail is coming from regulated source
       - See handout (i.e., existing LM317 regulator)
       - Disconnect *unregulated* DC supply from breadboard rails and connect to LM317 input
       - **Use 15 V_{DC} as *unregulated* input**
       - Connect LM317 output to breadboard rail so that LM317 powers entire breadboard
       - Regulated *bypass capacitors* (optional; see supplementary handout for details):
         - **LARGE bypass capacitor** (e.g., electrolytic) near LM317 output (and at Adjust)
         - **small bypass capacitor** (e.g., large ceramic) near 555 supply (i.e., 15 V_{DC} input)
     - (ii) **Next**, tune **duty cycle** so that $58.5\% \leq \Delta \leq 61.5\%$ by adjusting R_A and R_B
       - Increasing R_A increases duty cycle (and vice versa)
       - Increasing R_B decreases duty cycle (and vice versa)
       - Rather than changing resistances, sometimes it's easier to...
         - Increase resistance **slightly** by adding **small** resistors in **series**
         - Decrease resistance **slightly** by adding **large** resistors in **parallel**
     - (iii) **Last**, tune **frequency** f so that $30.0\,\text{kHz} \leq f \leq 32.8\,\text{kHz}$ by adjusting C (note: $C \propto 1/f$)
       - **Make frequency as LOW AS POSSIBLE!** (i.e., very close to 30 kHz)
       - To DECREASE f slightly, increase C **slightly** by adding **small** capacitors in **parallel**
       - To INCREASE f slightly, decrease C **slightly** by adding **large** capacitors in **series**
       - **REMEMBER** your tuned frequency for **calculations in next lab**