ECE 327: *Electronic Devices and Circuits Laboratory I*

Notes for Lab 4 (Oscillators Lab)

1. Introduce operational amplifiers

   - "Operational" and (historical) analog computers
     - Simulation of dynamical systems — think "SIMULINK"
     - Wider range of applications now
     - Simple integrators are still very influential
       - Switched-capacitor integrators make IC **state variable filters** cheap ("SC filters")
     - High-speed current-feedback (CFB) varieties available
   - Differential amplifier with **very high gain** (i.e., gain near ∞ or ∞/s)
   - Despite having same symbol, operational amplifiers are **NOT comparators**!
     - **Comparators** are *faster* (more like a *switch*) and can have special *switching* features
   - Example: non-inverting unity gain buffer (i.e., negative feedback and $A/(1+A)$)
     - Extension: "Superdiode" (i.e., "ideal" diode)
     - Op. amp. as integrator (i.e., from A to A/s) — input stage current driven into output *capacitor*
   - Real operational amplifiers (OAs)
     - PSRR (ripple rejection)
       - As in FET lab, power supply noise artifacts in output
     - Clipping *near* supply rails
       - Many OAs are not "rail-to-rail" (e.g., LM741) and may not even be symmetric
       - Oscillators depend on hard clipping
       - PSRR issues (solution discussed below)
     - Input leakage/bias current
       - Varies with input implementation
         - Tens of nanoamps bias with BJT-based (e.g., LM741)
         - Tens of picoamps leakage with BiJFET (e.g., LF351) — **can ignore**
         - Picoamps leakage with BiMOS (e.g., CA3130 and CA3160) — **can ignore**
       - Limits size of resistors (i.e., generate voltage drops)
       - Trim op. amp. to make input currents equal (e.g., OFFSET NULL pins, BALANCE pins, etc.)
       - Assuming trimmed inputs, try to keep resistance to ground equal at both inputs
     - Input impedance (i.e., Z_{in} between two inputs)
       - Varies with input implementation — similar to leakage
       - Is made nearly $\infty\,\Omega$ with *negative* feedback (i.e., op. amp. inputs are bootstrapped by output, so input-to-input current is forced to 0)
     - Slew rate — determined by maximum input stage current and output capacitance (I/C)
     - Temperature dependence
     - Parasitic capacitances — charging decreases bandwidth and stability margins
       - Cause: A few pF between every adjacent two pins (metal-air-metal capacitor)
       - Effect: Reduce bandwidth (phase effects can lead to instability in feedback loop)
       - Solution: Use small resistors and "larger" capacitors (to dominate parasitics) or frequency compensation (for feedback stability)

2. Oscillator building block: the ***multivibrator*** (**multi**ple discrete states leading to **multi**ple harmonics)
   - Two-state dynamic system characterized by long-term behavior (i.e., stability of *equilibria*)
     - **monostable**: returns to **single** equilibrium after moving into excited state for small time (e.g., camera button-iris action, oscilloscope "single shot")
     - **bistable**: returns to either of **two** stable equilibria depending on perturbation (e.g., latches, flip flops, comparators, *hysteresis*); usually has unstable Sisyphean equilibrium in between
     - **astable**: **no** stable equilibrium (e.g., clocks); bistable that is self-triggered
   - Oscillator implementation
     - operational amplifiers:
       * positive feedback Schmitt trigger (Otto H. Schmitt, biomedical engineering, squid nerves)
       * positive feedback makes $V+ = V-$ an *unstable node*
         · **bistable**: **Two** supply rails become **stable** equilibria
         · Switching occurs at $V+ = V-$ threshold crossing (*hysteresis*)
         · Fight poor PSRR with resistor-Zener-reneZ regulator (clipper) at output — matched double-anode-Zener-diode (DAZD) parts exist (i.e., two matched Zeners in one package)
     - 555 timer (e.g., LM555 or NE555): generates pulses with clever SR latch circuit
       * Output **s**ets when TRIGGER falls below $(1/3) \times V_{CC}$
       * Output unsets (i.e., **r**esets) when THRESHOLD rises above $(2/3) \times V_{CC}$
         · DISCHARGE is shorted to ground when output is unset
         · $(2/3) \times V_{CC}$ is tied to CONTROL (e.g., capacitively grounded for power-up unset)

3. Laboratory experience
   - When taking plots, save as CSV or BMP
     - Saving as BMP prevents extra work, but make sure scope plots show all required information
       * Intervals between horizontal and vertical divisions should be clear
       * In most cases, channel grounds should be shown
       * Channels should be labeled in report (e.g., "top waveform is input")
     - If saving CSV, **label axes**, **show units**, **identify waveforms** (e.g., "input", "output")
   - See pin-out handout
     - Operational amplifier **specificaitons** (e.g., expected *slew rates*)
     - Functional schematic of 555 timer circuit (shows *RS latch* and *comparators*)
   - **Follow lab *book* procedures**
     - See handout for more detailed instructions
     - In part 1, give slopes in V/μs units and compare to **slew rate** specification for each op. amp.
     - In part 2, use understanding of SR latch to explain results
     - In all parts, percent difference is
       $$\frac{\text{Measured} - \text{Expected}}{\text{Expected}} \times 100\%$$
     - After completing part 3, tune components for 30.0–32.8 kHz and 58.5–61.5% duty cycle
       * Tune frequency as close to 30 kHz as possible!
       * Keep tuned oscillator – will be used as clock in next lab
         · REMEMBER your tuned frequency for calculations in **next lab**

4. Laboratory reports
   - Answer all questions and provide all plots from lab procedures in lab text
   - For part 1, discuss problems caused by *finite slew rate* (see pin-outs for op. amp. specifications)
     - Slew rate impact on common negative-feedback configurations (e.g., inverting amplifier)?
   - For part 2, discuss problems caused by SR *latch* within 555 timer (triggering constraints?)