ECE 327: *Electronic Devices and Circuits Laboratory I*

Report Strategies for Lab 3 (Voltage Regulators Lab)

Abstract

This document outlines topics relevant to writing a report for this lab. Some theoretical models are presented that students can use to compare to measured results, and guidance is given on what content to present in the report.

Contents

1 General things to include in report

As with the rest of this document, each individual item **should not be answered like a question on a test**. Your answers **IN PARAGRAPH FORM** should cover these topics. A single sentence may address five or six bullets at once, whereas a whole paragraph may be needed for another bullet. Use these bullets to **guide your analysis**. **DO NOT ANSWER THEM DIRECTLY**.

Compare and contrast the four different regulators

- The off-the-shelf (OTS) LM317 regulator may be used as a benchmark.
  - How do the other regulators perform compared to it?
  - Does your laboratory data lead you to draw any conclusions about building your own *discrete* component regulators (as opposed to purchasing an *integrated circuit (IC)* regulator)?
  - In practice, why do we favor an IC regulator (like the LM317) over a discrete transistor regulator?
- *Quiescent current (QC)* represents the **additional current** that the regulator requires to operate (i.e., the *operating current*).
  - What components contribute the most to the QC?
  - Even if a current limiter (or foldback circuit) could be built for *free* that had *no negative impact* on regulation, is there a reason why you might *not* include it in your regulator design? Is there a *cost* for the extra *complexity*?
  - How does the LM317 compare?
- The *dropout (DO) voltage* is the minimum voltage that must be dropped *across* a regulator for it to operate properly. That is, it's the minimum difference between input and output voltages.
  - What elements contribute to the DO? Why?
  - The R_{CL} and R_S resistors are called *sense* resistors because they *sense* current. How do they *sense* current? How do they contribute to DO?
    - Note that the LM317 DO strongly depends on output current while output voltage does not.
  - Temperature has an impact on the DO of our circuits (as it often does). Why?
    - Note that the LM317 DO strongly depends on temperature while output voltage does not.
    - Note that *both* output voltage *and* current limit of the LM317 do *not* depend on temperature.
- Compare regulation characteristics (e.g., in one table or plot).
  - What is relationship between **line regulation of Zener and discrete transistor regulator**?
    - How does regulation compare in V/V units? Why?
    - How does regulation compare in %/V units? Why?
    - Why use different units?
    - Will using a different Zener diode affect line regulation? How?
    - Can the line regulation of the discrete transistor regulators be improved by changing how the Zener diode is connected to the circuits? How?
  - The discrete transistor regulator load regulation curves reflect the exponential transconductance curves of a bipolar transistor. So it *may* be instructive to use *semi-log* plots of your data (especially when *extrapolating* short-circuit behavior).
  - *Hot* resistors can have increased resistance. How could this affect your i_{out} estimates?
  - How does current limiting and foldback affect load regulation?
  - Discrete transistor regulation without current limiting/foldback has near perfect load regulation. Why add limiting/foldback?
  - What are the advantages of current foldback over simple current limiting?

2 Things to include for Zener shunt regulator

Overall goal is to show me that you understand the operation of Zener diodes and how their characteristics impact important voltage regulator specifications.

1. Identify **which Zener diode** was used (e.g., 1N4731, 1N5229, or 1N751).
2. Identify **calculated** R_Z.
   - If circuit output with calculated R_Z was not desired, describe how.
   - You should *not* have tuned your circuit. You should compare your results with what you expected and suggestion reasons for any differences.
3. Compare **measured results** to **theoretical results**.
   - A brief explanation of a theoretical model of our circuit is given in Appendix A.
   - From model in Appendix A, the expected output

$$v_{\text{out}} = \begin{cases} v_{\text{in}} \frac{L}{R_Z+L} & \text{if } v_{\text{in}} \frac{L}{R_Z+L} \leq (V_Z - I_Z R_{\text{on}}), \\ v_{\text{in}} \frac{R_{\text{on}} \| L}{R_{\text{on}} \| L + R_Z} + (V_Z - I_Z R_{\text{on}}) \frac{R_Z \| L}{R_{\text{on}} + R_Z \| L} & \text{otherwise.} \end{cases}$$

     - Use expression to compare measured and expected **line regulation**.
       - Vary v_{in} and predict v_{out}.
       - Plot predicted v_{in}–v_{out} curve for comparison with measured curve.
       - Give % error between measured and expected line regulation (in both V/V and %/V units) and (approximate) PSRR ratio.
     - Use expression to compare measured and expected **load regulation**.
       - Vary L and predict v_{out}.
       - Plot predicted L–v_{out} (or i_{out}–v_{out}) curve for comparison with measured curve.
       - Give % error between measured and expected load regulation.
     - If not possible to plot measured and expected results on *same* axes, plot them separately using **same scaling and limits**. **THIS RULE GOES WITHOUT SAYING.**
   - Expected operating or *quiescent* current (from model in Appendix A)

$$QC \approx \begin{cases} 0 & \text{if } v_{\text{in}} \frac{L}{R_Z+L} \leq (V_Z - I_Z R_{\text{on}}), \\ \frac{v_{\text{out}} - (V_Z - I_Z R_{\text{on}})}{R_{\text{on}}} & \text{otherwise.} \end{cases}$$

     - Use expression to compare measured and expected **quiescent current (QC)**.
       - Vary L and predict QC.
         - In QC expression, either use v_{out} from theory, v_{out} from measurements, or both.
         - Report your method.
       - Plot predicted L-QC (or i_{out}-QC or v_{out}-QC) curve for comparison with measured curve.
     - Same scaling rule as before applies.
   - Expected **dropout (DO) voltage** is

$$(V_Z - I_Z R_{\text{on}}) \frac{R_Z}{L}$$

     - Discuss differences from measured DO.
       - Is DO easy to measure?
       - Why is this DO expected? Does the model perform well (i.e., model reality) in this region?

3 Things to include for discrete-transistor regulators

The following are approximations. **If they vary greatly from data, try the more exact expressions from Appendix B.**

1. Identify **all calculated values** for all resistors in schematic (i.e., R_Z, R_1, R_2, R_{CL}, R_S, R_3, and R_4).
2. Compare **measured results** to **theoretical results**.
   - Both discrete-transistor regulators operate like the simplified circuit in Appendix B.
     - The regulator starts regulating when
     $$v_{\text{in}} \geq \left(1 + \frac{R_1}{R_2}\right)\left((V_Z - I_Z R_{\text{on}}) + \overbrace{0.65\,\text{V}}^{\text{From } Q_R}\right) + \overbrace{0.65\,\text{V}}^{\text{From } Q_C},$$
     where the Q_C 0.65 V will be closer to 0.5 V as Q_C heats up. So the **DO voltage** is ∼0.65 V, which is the base–emitter drop across the Q_C transistor.
     - In the *subregulation region* (i.e., before the regulator starts regulating),
     $$v_{\text{out}} \approx \begin{cases} 0 & \text{if } v_{\text{in}} \leq 0.65\,\text{V}, \\ v_{\text{in}} - 0.65\,\text{V} & \text{otherwise.} \end{cases}$$
     - In the *regulation region*,
     $$v_{\text{out}} = \left(1 + \frac{R_1}{R_2}\right)\left(v_{\text{in}}\left(\frac{R_{\text{on}}}{R_{\text{on}}+R_Z}\right) + (V_Z - I_Z R_{\text{on}})\frac{R_Z}{R_{\text{on}}+R_Z} + 0.65\,\text{V}\right).$$
     - As before, **compare measured curves with expected curves**; try to explain differences.
     - Do you have thoughts on how connecting R_Z to v_{out} instead of v_{in} could change your results?
   - The *quiescent current (QC)* is the regulator current that is not delivered to the load.
     - Assuming R_{CL} and R_{on} are very small, a good approximation of the current-limited QC is
     $$\overbrace{\frac{v_{\text{in}} - V_Z}{R_Z} + \frac{v_{\text{in}} - (v_{\text{out}} + 0.65\,\text{V})}{1\,\text{k}\Omega}}^{I_Z} + \overbrace{\frac{v_{\text{out}}}{R_1 + R_2}}^{\text{Divider Current}}.$$
     - Assuming R_S and R_{on} are very small, a good approximation of the current-foldback QC is
     $$\frac{v_{\text{in}} - V_Z}{R_Z} + \frac{v_{\text{in}} - (v_{\text{out}} + 0.65\,\text{V})}{1\,\text{k}\Omega} + \frac{v_{\text{out}}}{(R_1 + R_2) \parallel (R_3 + R_4)}.$$
     Compare your QC data with what is expected.
   - The current limiting/foldback circuit in series with the output will eventually activate[1] and cause measurements to deviate from non-limited model[2].
     - In the *current-limited case*, Q_{CL} *starts* to activate when its base–emitter drop reaches ∼0.5 V. So deviations are expected to start at $i_{\text{out}} \approx (0.5\,\text{V})/R_{CL}$ (i.e., at $L \approx R_{CL} \times (10\,\text{V})/(0.5\,\text{V})$).
       - When does the limiter start to activate in your circuit? Expected?
       - From your data, predict i_{out} for $L = 0\,\Omega$ (i.e., i_{SC}). Expected?
     - For the *current-foldback* case, the Q_{FB} transistor *starts* to activate when its base–emitter drop reaches ∼0.5 V, or when
     $$i_{\text{out}} \approx \frac{(10\,\text{V})\frac{R_3}{R_3+R_4} + 0.5\,\text{V}}{R_S\frac{R_4}{R_3+R_4}} \qquad \text{(i.e., when} \qquad L \approx \frac{R_S\frac{R_4}{R_3+R_4}}{\frac{R_3}{R_3+R_4} + \frac{0.5\,\text{V}}{10\,\text{V}}} \qquad \text{)}.$$
       - When does the foldback limiter start to activate in your circuit? Expected?
       - From your data, predict i_{FB} and i_{SC}. Expected?

[1] A diode *starts* to pass current at its so-called "*cut-in voltage*," which is ∼0.5 V for a Silicon diode at room temperature.
[2] Note that *hot resistors* can have increased resistance. How might this fact affect your i_{out} estimates from data?

4 Things to include for LM317 regulator

There is little analysis that can be done on the off-the-shelf (OTS) LM317 regulator. However, we can use it as an example of an industry-class regulator and compare its performance with the regulators we built in class.

1. **Report calculated** R_1 and R_2 values for the regulator.
2. Compare **measured results** to **expected results**.
   - You measured the difference between the output and adjust pins. Was it 1.25 V?
3. Compare performance of LM317 with the other three regulators.
   - Are there noticeable improvements? Explain.
   - This regulator can deliver up to 1.5 A of current to a load without damaging *itself*. After that, its own *internal* current limiters activate. Is there any reason why we might want additional current limiting? We limited short-circuit current to protect the *regulator*. However, if the regulator can provide lots of current without damaging *itself*, are there other reasons to limit short-circuit current?
     - The LM317 datasheet includes a sample application that adds a current limiter to the LM317 output. Why would an external limiter be desirable?
       * The LM317 datasheet also includes examples that use *external pass transistors* to provide *more* than its maximum 1.5 A of current.
       * External *foldback* limiting can also be added.
     - Why might having the ability to add a current-limiting (or current-foldback) circuit *externally* to the LM317 be attractive?
       * How do you think the additional circuit might affect the DO voltage?
       * How do you think the additional circuit might affect the load regulation?
     - Do you think the large piece of metal extending from the package of the LM317 has anything to do with its ability to deliver high output current?
       * The piece of metal acts as a *heat sink* which helps transfer *heat* from the part to the outside air more efficiently (i.e., more energy transfer per unit time). Adding more metal surface area results in more heat exchange.
         · The LM317 has a hole in its heat sink that is often used to attach it (e.g., with a metal screw) to a large piece of metal (e.g., the chassis/case of a bigger device). Why?
         · Why do you think large computer heat sinks have lots of fins?
         · Sometimes a paste called "heat sink compound" is used between semiconductors and their heat sinks (or heat sinks and larger pieces of metal). Among other things, this compound fills in cracks between the two materials and evacuates any air between them. What do you think its purpose is?
       * *Heat* and *temperature* are analogous to *current* and *voltage*, respectively. For example, objects with high *heat capacity* (related to "*specific heat*") are like capacitors with high *capacitance*; it takes a lot of heat to change their temperature.
         · "Thermal resistances" are sometimes used in "thermal circuits."
         · "Thermal circuits" are usually driven by "current sources" that represent heat sources.
         · Thermal circuits are frequently used by IC and power engineers. Why?
       * An object can be damaged by high *temperatures*, and *heat* provides a mechanism to raise temperatures. If heat can be evacuated, temperatures can be stabilized, and damage can be avoided.
4. What is another performance advantage of the LM317 that we *did not* test in this laboratory? (hint: it's a *bandgap reference*)
5. Comment on reasons why we'll use the LM317 circuit for our project.

A Linear Model of Zener Regulator Circuit

- The **linear model** of reverse-biased Zener uses a DC voltage source with series resistance (parameter values given on **parts handout**).
  - Voltage: $V_Z - I_Z R_{\text{on}}$
  - Series resistance (i.e., incremental resistance): R_{on}

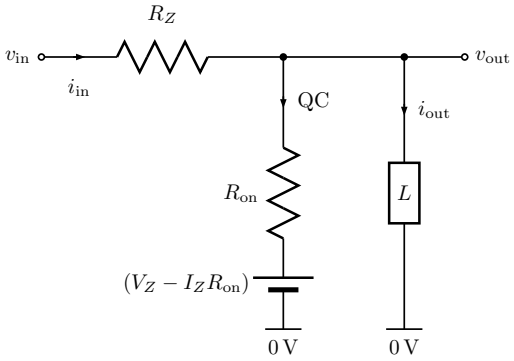
  In particular, a reverse-biased Zener like

  and has an i–v curve modeled (for $v > 0$) by

$$i(v) \approx \begin{cases} 0 & \text{if } v < (V_Z - I_Z R_{\text{on}}), \\ \frac{v_Z - (V_Z - I_Z R_{\text{on}})}{R_{\text{on}}} & \text{otherwise.} \end{cases}$$

  So if $R_{\text{on}} = 0$, the curve is a right angle with vertex at $v = V_Z$. For any R_{on}, $i(V_Z) = I_Z$, as desired.

- In our regulator, if Zener voltage reaches $V_Z - I_Z R_{\text{on}}$, the Zener passes current, and the circuit becomes



  Using *superposition*, the transfer function is

$$v_{\text{out}} = v_{\text{in}} \frac{L \| R_{\text{on}}}{R_Z + L \| R_{\text{on}}} + (V_Z - I_Z R_{\text{on}}) \frac{R_Z \| L}{R_{\text{on}} + R_Z \| L} \qquad \text{where} \qquad x \| y \triangleq \frac{xy}{x+y}.$$

  Otherwise, if the Zener voltage is less than $V_Z - I_Z R_{\text{on}}$, the circuit is a simple R_Z–L divider where

$$v_{\text{out}} = v_{\text{in}} \frac{L}{R_Z + L}.$$

  Combining these two, we have

$$\boxed{v_{\text{out}} = \begin{cases} v_{\text{in}} \frac{L}{R_Z + L} & \text{if } v_{\text{in}} \frac{L}{R_Z + L} \le (V_Z - I_Z R_{\text{on}}), \\ v_{\text{in}} \frac{L \| R_{\text{on}}}{R_Z + L \| R_{\text{on}}} + (V_Z - I_Z R_{\text{on}}) \frac{R_Z \| L}{R_{\text{on}} + R_Z \| L} & \text{otherwise.} \end{cases}}$$

  In other words, a low R_{on} shorts out contribution from v_{in} and replaces it with $(V_Z - I_Z R_{\text{on}})$.

- The operating current, or ***quiescent* current**, is the current through the Zener. That is,

$$\boxed{QC \approx \begin{cases} 0 & \text{if } v_{\text{in}} \frac{L}{R_Z + L} \le (V_Z - I_Z R_{\text{on}}), \\ \frac{v_{\text{out}} - (V_Z - I_Z R_{\text{on}})}{R_{\text{on}}} & \text{otherwise.} \end{cases}}$$

- The **dropout (DO) voltage** should be $(V_Z - I_Z R_{\text{on}})(R_Z / L)$, which is the difference between v_{in} and v_{out} at the "**instant**" the Zener "activates." Is "*instant*" realistic?

B Analysis of Discrete Transistor Regulator Circuit

Both discrete transistor regulators are based on the simpler *Discrete Transistor Adjustable Series Voltage Regulator* that is discussed in the procedure text. In this regulator,

- The Q_C transistor is called a *pass transistor* because it passes current from input to output. As its collector and emitter are essentially *in series* with the output, it serves to dissipate the additional energy to keep v_{out} regulated.
- The Q_R transistor is called a *regulation transistor* because its base *senses* the output (scaled by the R_1–R_2 resistor) and controls the Q_C transistor in order to maintain the right output level.

The regulation circuit should be analyzed in two cases. In both cases, the R_Z resistor biases the Zener diode into its "on" region so that it maintains V_Z across it. However, in the *subregulation region*, the Q_R resistor is in cutoff and has no impact on the circuit. It turns on in the *regulation region*.

Regulation Region

In the regulation region,

$$v_{\text{out}} = (v_Z + 0.65\,\text{V})\left(1 + \frac{R_1}{R_2}\right)$$

where v_Z is the voltage across the Zener diode, or (using reasoning from Appendix A)

$$v_Z = v_{\text{in}}\frac{R_{\text{on}}}{R_{\text{on}} + R_Z} + (V_Z - I_Z R_{\text{on}})\frac{R_Z}{R_{\text{on}} + R_Z} + (v_{\text{in}} - v_{\text{out}} - 0.65\,\text{V})\frac{R_Z \| R_{\text{on}}}{1\,\text{k}\Omega}$$

where R_{on}, V_Z, and I_Z are given in the parts handout. Together, in the regulation region,

$$v_{\text{out}} = \left(v_{\text{in}}\left(\tfrac{R_{\text{on}}}{R_{\text{on}}+R_Z} + \tfrac{R_Z \| R_{\text{on}}}{1\,\text{k}\Omega}\right) + (V_Z - I_Z R_{\text{on}})\tfrac{R_Z}{R_{\text{on}}+R_Z} - (v_{\text{out}} + 0.65\,\text{V})\tfrac{R_Z \| R_{\text{on}}}{1\,\text{k}\Omega} + 0.65\,\text{V}\right)\left(1 + \tfrac{R_1}{R_2}\right)$$

or

$$\boxed{v_{\text{out}} = \left(\frac{1\,\text{k}\Omega}{\frac{R_2}{R_1+R_2}(1\,\text{k}\Omega) + R_Z \| R_{\text{on}}}\right)\left(v_{\text{in}}\left(\tfrac{R_{\text{on}}}{R_{\text{on}}+R_Z} + \tfrac{R_Z \| R_{\text{on}}}{1\,\text{k}\Omega}\right) + (V_Z - I_Z R_{\text{on}})\tfrac{R_Z}{R_{\text{on}}+R_Z} + (0.65\,\text{V})\left(1 - \tfrac{R_Z \| R_{\text{on}}}{1\,\text{k}\Omega}\right)\right).}$$

Load regulation and power dissipation

In this model, the output voltage does not depend on L. That is, if we assume that $\beta L \gg 1\,\text{k}\Omega$, the base current into Q_C will be negligible, and the circuit will have excellent (i.e., very low) *load regulation*. However, power dissipation in the Q_C pass transistor can rise to dangerously high levels. Power dissipation for this circuit is given by $(v_{\text{in}} - v_{\text{out}})i_{\text{out}}$, and so it rises linearly with output current and is *not* bounded.

Line regulation

Next, if we can assume that $R_Z \| R_{\text{on}} \ll 1\,\text{k}\Omega$, then

$$v_{\text{out}} \approx \left(v_{\text{in}}\frac{R_{\text{on}}}{R_{\text{on}} + R_Z} + (V_Z - I_Z R_{\text{on}})\frac{R_Z}{R_{\text{on}} + R_Z} + 0.65\,\text{V}\right)\left(1 + \frac{R_1}{R_2}\right).$$

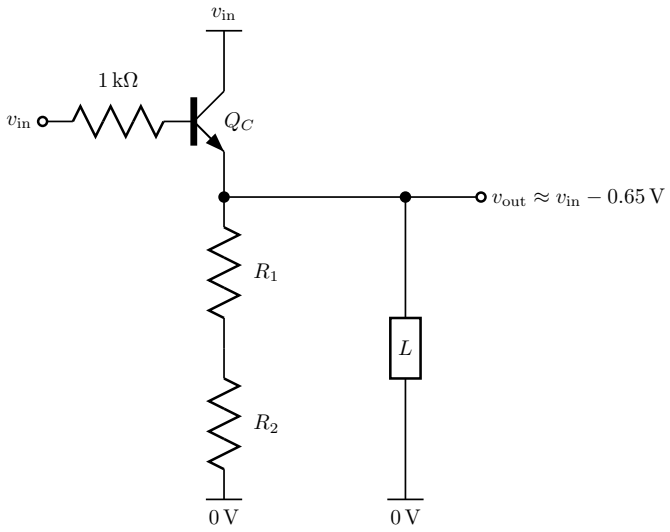
If it is also the case that L is relatively large compared to R_Z and R_{on}, then the *line regulation* of the discrete transistor regulator (when measured in V/V) will be equal to the line regulation for the Zener regulator after being scaled by $(1 + R_1/R_2)$. That is, the R_1–R_2 divider applies *gain* to the Zener diode, and so any dependence it has on v_{in} is *magnified* in the discrete transistor regulator's output. However, the line regulation in %/V units should be equal to or better (i.e., less) than the %/V line regulation of the Zener. That is, the output voltage increases by roughly the same amount as the V/V line regulation, so the %/V numbers should be roughly the same.

Subregulation Region

The regulation transistor Q_R will not activate until its base is approximately 0.65 V above its emitter. Hence, the *subregulation region* is where

$$\overbrace{v_{\text{out}}\frac{R_2}{R_1+R_2}}^{Q_R\text{ base}} \le \overbrace{v_{\text{in}}\frac{R_{\text{on}}}{R_{\text{on}}+R_Z}+(V_Z-I_ZR_{\text{on}})\frac{R_Z}{R_{\text{on}}+R_Z}}^{Q_R\text{ emitter}}+0.65\,\text{V}$$

During this region, the Q_R resistor can be ignored, and so the circuit becomes



As long as $1\,\text{k}\Omega \ll \beta((R_1+R_2)\|L)$, the pass transistor Q_C sees v_{in} at its base. So

$$\boxed{v_{\text{out}} \approx \begin{cases} 0 & \text{if } v_{\text{in}} \le 0.65\,\text{V}, \\ v_{\text{in}} - 0.65\,\text{V} & \text{otherwise.} \end{cases}}$$

However, because Q_C carries much current, due to excessive heat dissipation in the transistor, the 0.65 V base–emitter drop may reduce to as little as 0.5 V depending on the load. Hence, the subregulation region is the region where

$$0\,\text{V} \le v_{\text{in}} \le \left(v_{\text{in}}\frac{R_{\text{on}}}{R_{\text{on}}+R_Z}+(V_Z-I_ZR_{\text{on}})\frac{R_Z}{R_{\text{on}}+R_Z}+\overbrace{0.65\,\text{V}}^{\text{From } Q_R}\right)\left(1+\frac{R_1}{R_2}\right)+\overbrace{0.65\,\text{V}}^{\text{From } Q_C},$$

or

$$\boxed{0\,\text{V} \le v_{\text{in}} \le \frac{1}{\frac{R_2}{R_1+R_2}-\frac{R_{\text{on}}}{R_{\text{on}}+R_Z}}\left((V_Z-I_ZR_{\text{on}})\frac{R_Z}{R_{\text{on}}+R_Z}+0.65\,\text{V}\right)+(0.65\,\text{V})\frac{R_2(R_{\text{on}}+R_Z)}{R_2R_Z-R_1R_{\text{on}}}.}$$

Dropout (DO) Voltage

If we assume that $R_{\text{on}} \ll R_Z$, then the approximate subregulation region is

$$0\,\text{V} \le v_{\text{in}} \le \left(1+\frac{R_1}{R_2}\right)((V_Z-I_ZR_{\text{on}})+0.65\,\text{V})+0.65\,\text{V} \approx v_{\text{out}}+0.65\,\text{V}.$$

That is, at the instant the regulator enters its regulation region, the difference $v_{\text{in}}-v_{\text{out}}$ is 0.65 V (or ∼0.5 V for hot Q_C transistors). So 0.65 V should approximate the actual DO voltage well.

Current Limiting and Current Foldback

Adding current limiting or current foldback has little impact on the circuit during normal operation.

No Limiting Case

In the case where neither current limiting nor foldback is implemented, the output v_{out} is constant while the input v_{in} is in the regulation region. In this case, the operating current, or **quiescent current (QC)**,

$$\text{QC} = \overbrace{\frac{v_{\text{in}} - V_Z}{R_Z} + \frac{v_{\text{in}} - (v_{\text{out}} + 0.65\,\text{V})}{1\,\text{k}\Omega}}^{I_Z} + \overbrace{\frac{v_{\text{out}}}{R_1 + R_2}}^{\substack{\text{Divider}\\ \text{Current}}}.$$

That is, the *operating current* consists of the current through the Zener diode and the current through the R_1–R_2 feedback gain network.

Current-Limiting Case

When the current limiter is added, the drop across R_{CL} slightly changes the Zener current. So the **quiescent current**

$$\boxed{\text{QC} \approx \frac{v_{\text{in}} - V_Z}{R_Z} + \frac{v_{\text{in}} - \left(v_{\text{out}}\left(1 + \frac{R_{CL}}{L\|(R_1+R_2)}\right) + 0.65\,\text{V}\right)}{1\,\text{k}\Omega} + \frac{v_{\text{out}}}{R_1 + R_2}.}$$

That is, the voltage seen at the emitter of Q_C is slightly higher to account for the small drop across R_{CL}. This model of QC does not account for the impact of $R_{\text{on}} \neq 0$. That is, as the Q_C emitter current rises, the current through the Zener should *decrease*. Assuming that R_{on} is small and that most of the Zener biasing current is delivered via R_Z, the Zener potential at the emitter of Q_R should not change much, and so this expression should be a good approximation.

Also, in the current-limiting case, the output v_{out} will cease to be constant when the Q_{CL} transistor starts turning on, which occurs when its base–emitter diode reaches ∼0.5 V (i.e., the room-temperature *cut-in voltage* for a Silicon diode). So we expect current limiting to make an impact on output (i.e., by reducing output voltage) near

$$\boxed{i_{\text{out}} \approx \frac{0.5\,\text{V}}{R_{CL}}} \quad \text{(i.e., when} \quad \boxed{L \approx \frac{10\,\text{V}}{0.5\,\text{V}} R_{CL}} \quad \text{).}$$

Current-Foldback Case

When the current limiter is replaced with the current foldback circuit, resistor R_S has the same impact as the old R_{CL} on the Q_C emitter, but *additional* current drives the new R_3–R_4 divider. So the **quiescent current**

$$\boxed{\text{QC} \approx \frac{v_{\text{in}} - V_Z}{R_Z} + \frac{v_{\text{in}} - \left(v_{\text{out}}\left(1 + \frac{R_S}{L\|(R_1+R_2)}\right) + 0.65\,\text{V}\right)}{1\,\text{k}\Omega} + \frac{v_{\text{out}}}{R_1 + R_2} + \frac{v_{\text{out}}\left(1 + \frac{R_S}{L\|(R_1+R_2)}\right)}{R_3 + R_4}.}$$

As long as R_S is small compared to $L\|(R_1 + R_2)$, the R_1–R_2 divider and the R_3–R_4 divider can be viewed as being in parallel with each other. In either case, the approximation does not account for $R_{\text{on}} \neq 0$. However, assuming $R_{\text{on}} \approx 0$ and that most Zener biasing current comes via R_Z, the QC should be modeled well by this expression.

Output current will start to **fold back** when the Q_{FB} transistor starts to active, which occurs when its base–emitter drop reaches ∼0.5 V. Hence, assuming v_{in} puts the regulator into its regulation region, a foldback effect (e.g., sinking output voltage) should start to occur near

$$\boxed{i_{\text{out}} \approx \frac{v_{\text{out}}\frac{R_3}{R_3+R_4} + 0.5\,\text{V}}{R_S\frac{R_4}{R_3+R_4}}} \quad \text{(i.e., when} \quad \boxed{L \approx \frac{R_S\frac{R_4}{R_3+R_4}}{\frac{R_3}{R_3+R_4} + \frac{v_{\text{out}}}{0.5\,\text{V}}}} \quad \text{)}$$

where v_{out} is the constant regulated voltage from the regulation region (e.g., 10 V).