ECE 327: *Electronic Devices and Circuits Laboratory I*

Procedure Notes for Lab 2 (Field Effect Transistor Lab)

Abstract

The laboratory procedure is broadly outlined in the lab *book*. You are expected to gather all data and answer all questions required by that text. Here, some additional details are presented that should help you build your circuits.

Contents

Laboratory Pacing: Quick–Quick–Slow

The first two parts of this laboratory can be completed fairly quickly. They involve simple circuits that use few components and are easy to operate. While the third section is an extension of the second section, it may take substantially longer than the either of the first two sections. Move quickly through the first two sections so you can take your time carefully setting up the third section.

CMOS Parts: Be Careful

The CMOS parts used in this laboratory are very delicate. Keep several things in mind when using them.

(i) Be careful when installing these parts, which are susceptible to damage from SCR latch-up and ESD.

- Keep some part of your skin in direct contact with a metallic portion of your breadboard.
- Make sure power is turned **OFF** during installation, and connect all power rails *first*.
- Keep input signal turned **OFF** until *after* powering up circuit.
- *Before* powering down circuit, turn input signal **OFF**.

(ii) Some chips from the cabinet implement several components on one part (e.g., a single CD4066 implements four switches). One of these components to be damaged while another component works fine. So if you find one particular component does not appear to be working properly (e.g., one FET switch that is stuck *on*), try using another component on that same part before getting a new part.

(iii) If you have problems with your circuit, setup simple test circuits to make sure each chip is operating properly. If one component on a chip isn't working, try using a different component on the same chip.

Laboratory Goals: Parts and Principles

(i) Understand how to use (and test) the CD4066 FET switch.

(ii) Understand how to use (and test) the CD4049 CMOS inverter.

(iii) Understand the effect of driving a constant current into a capacitor and how this relates to integration.

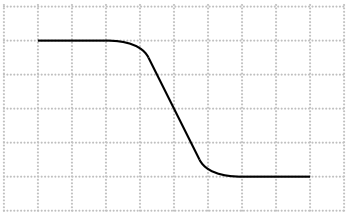
(iv) Understand how last two sections are related (i.e., how/why to use a switched capacitor as a resistor).

1 CMOS Inverter (*class-A* CMOS linear inverting amplifier)

- See Figure 2.5 from lab book for schematic of CMOS inverter.
- Part CD4007 provides several FETs that can be used to build the CMOS inverter.
- See pin-outs handout or page 2.10 of the lab book for CD4007 information.
  - For example, shorting pins 8 and 13 creates a CMOS inverter with pin 6 input and pin 8 output.
  - **Make sure** to provide supply rails to bulk pins 7 and 14
    - $V_{DD} = V+ = 5\,\text{V}$ (pin 14)
    - $V_{SS} = V- = -5\,\text{V}$ (pin 7)
- Use oscilloscope's X–Y mode to find input-to-output transfer function of inverter.
  - Generate a *slow* (e.g., 60 Hz) triangle wave that goes from $-5\,\text{V}$ to $5\,\text{V}$.
  - Use triangle wave as inverter's input.
  - Also connect triangle wave (v_{in}) to channel 1 (i.e., X).
  - Connect inverter's output (v_{out}) to channel 2 (i.e., Y).
  - Press the `Main` button in the `Horizontal` section of buttons at the top of the scope.
  - Press the `XY` soft button on the screen to put the scope into X–Y mode.
  - Plot may be improved by using `Averaging` under `Acquire`.

  In X–Y mode, at each instant, a single point is plotted with channel 1 data as its X coordinate and channel 2 data as its Y coordinate. Tune triangle wave to slower frequency (e.g., 1 Hz) to see the effect.
  - Triangle wave (i.e., X channel) sweeps through all possible inputs.
  - Inverter output is shown in Y channel.
  - Turning on `∞ Persist` under `Display` causes draws a trail showing history.

  The resulting graph is "Z"-shaped:



  Use *cursors* to determine the quantities requested in the text. In some cases, it will be easier to change the scope back to `Normal` mode. **SAVE PLOT (with *Gain* cursors shown) FOR REPORT.**
  - **High** and **low** voltage levels are Y value at top and bottom of the "Z".
  - **Inverter threshold** is the range of input voltages where device acts like an *inverter* (i.e., sides).
  - **Linear range** is range of input voltages where inverter acts like linear amplifier (i.e., middle).
  - **Gain** of transition region is slope of linear portion in middle of the "Z".

Class A, Class B, Power, and Distortion

In its linear range, the CMOS inverter acts like a *class-A amplifier*. Both MOSFETs are in their "active" mode, and so current can flow from V_{DD} to V_{SS}, which will cause power dissipation in both FETs at all times. Because *both* transistors are always conducting, this amplifier is said to be in *class A*. These amplifiers produce a high fidelity output at the cost of maximal power dissipation. The push–pull amplifier built in the BJT lab is a *class-B* amplifier because only one transistor conducts current at a time, and so it "wastes" less power at the cost of increased distortion (i.e., *crossover distortion*).

2 Continuous-Time Integrator

- The supplementary text on continuous-time integrators has **schematics,** formulas, and explanations.
- Build a continuous-time integrator. See supplementary text for **schematic** and more information.
  - **Operational amplifier**: fast JFET-input LF351 (**instead of** slow/leaky LM741 from lab book)
  - Feedback capacitor: 0.01 μF (10 nF = 10 000 pF, so capacitor code is `103`)
  - Inverting input (i.e., "−" input) resistor: 10 kΩ (resistor code: `brown`–`black`–`orange` or `103`)
  - Supply rails: ±6 V (at *least*)
  - **To help with offset**, connect non-inverting input (i.e., "+" input) to ground via a 10 kΩ resistor.
    - That is, use a 10 kΩ resistor instead of a short-circuit connection.
      - Ideally, current into the input is 0 A, and so the resistor is equivalent to a short circuit.
    - Use 10 kΩ because the inverting input (i.e., "−" input) sees 10 kΩ.
    - Assuming the leakage to both inputs is **equal**, the resistor cancels any offset.
    - A tunable 10 kΩ (e.g., a variable resistor) provides flexibility.
- Generate square wave input with function generator:
  - Amplitude: 2.5 V (i.e., 5 $V_{\text{peak-to-peak}}$)
  - Frequency: 1 kHz
  - Offset: 0 V (IMPORTANT TO BE PRECISE!)
    - **Old generators:** Use −20 dB offset button to minimize offset.
    - **New generators:** Use highest precision units (e.g., μV) to minimize offset.
- Plot the input and output on the same graph using the oscilloscope.
- Because it is the integral of a square wave, the output wave should look **triangular**. **Find its slope** (e.g., use `Cursors` to find $\Delta Y/\Delta X$).
  - **UNEXPECTED OUTPUT OFFSETS:** Your output may drift or have significant DC offset. See the supplementary text for an explanation. **Comment on these effects in your report.**
    - You may attempt some of the strategies in the supplementary document.
    - **QUICK FIX**: Try adjusting the non-inverting input (i.e., "+" input) resistance to ground.
  - **CLIPPING OF OUTPUT:** Because the output may have a significant offset, it's possible that the op. amp. output will attempt to move outside of the supply rails, which will cause *clipping*.
    - **Make sure your input signal has a 2.5 V amplitude and *not* a 5 V amplitude**.
    - **Make sure** your input signal has a 0 μV_{DC} offset.
    - Adjust value of non-inverting input (i.e., "+" input) resistor to ground.
    - Increasing the op. amp. supply rails may reduce clipping.
    - To decrease additional clipping, adjust input offset slightly until output is *nearly* triangular.
      - Some small noise at vertices of triangles is acceptable.
- **SAVE A PLOT** that shows both the input and output on the same screen.
  - Position `Cursors` to measure ΔY and ΔX so you can calculate triangle wave slope.
  - Save the plot **with slope cursors shown**.
- Use supplementary text to derive expected slope of output wave.
- **DO NOT** disassemble the circuit! It is used in the next part!

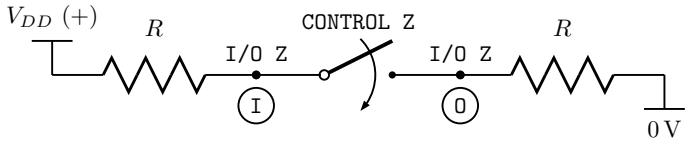
In your report, compare observed and expected results.

3 Switched-Capacitor Integrator

Here, the 10 kΩ resistor from your continuous-time integrator is replaced with a *switched-capacitor (SC) resistor*. The SC resistor is made from two FET switches, a capacitor, and a fast clock (from an LM555 or NE555 timer circuit). On an *integrated circuit*, silicon area is costly, and so SC resistors are cheaper than simple resistors because they are much smaller. Also, SC resistances can be matched and tuned externally by adjusting a clock frequency, but they add complexity and a clock that may introduce noise.

DO NOT BUILD YOUR ENTIRE CIRCUIT AT ONCE. Follow the steps below.

1. Build the astable timer circuit shown in Figure 2.10 in the lab book. The output is signal CLK.
   - The output is a square wave with period T.
     - Use clock frequency $f_{CLK} = 100\,\text{kHz}$ (SC rule of thumb: switch at 10× input frequency).
     - **SOLVE** FOR R_a so that $T = 1/f_{CLK}$. Because $R_b = 4R_a$, $T = 9R_aC\ln(2)$.
     - Use capacitor $C = 1\,\text{nF}$ ($1\,\text{nF} = 1000\,\text{pF}$, so capacitor code is `102`).
     - Solve for ideal R_a (and $R_b = 4R_a$).
   - Build **and test** clock circuit.
     - Timer IC: LM555 or NE555 (i.e., "555")
     - Supply rails at ±6 V as before (at *least*).
       - $V+ = HIGH = V_{CC} = 6\,\text{V}$ and $V- = LOW = V_{EE} = -6\,\text{V}$ (NOT 0 V)
     - Tune C until $95\,\text{kHz} \le f_{CLK} \le 105\,\text{kHz}$.
       - If $f_{CLK} \approx 80\,\text{kHz}$, try adding **two** 0.01 μF (cap. code: `103`) capacitors *in* ***series*** with C.
       - If $f_{CLK} \approx 90\,\text{kHz}$, try adding **one** 0.01 μF (cap. code: `103`) capacitor *in* ***series*** with C.
2. Use CD4049 inverter to generate $\overline{CLK}$.
   - **DO NOT** use the CD4007 from the first part of the lab.
   - Use same ±6 V supply rails as before.
     - $V+ = HIGH = V_{DD} = 6\,\text{V}$ and $V- = LOW = V_{SS} = -6\,\text{V}$ (NOT 0 V)
   - **TEST INVERTER BEFORE CONNECTING TO** CLK.
     - Connect V_{DD} and V_{SS}.
     - Connect inverter input to V_{DD} and use DMM to make sure output is V_{SS}.
     - **RE**connect inverter input to V_{SS} and use DMM to make sure output is V_{DD}.
     - Repeat until you find **one** working inverter. You may have to try all six on your chip.
   - **RE**connect inverter input to CLK signal. Probe to make sure output is $\overline{CLK}$.
3. Use CD4066 for two switches.
   - Use ±6 V supply rails ($V+ = HIGH = V_{DD} = 6\,\text{V}$ and $V- = LOW = V_{SS} = -6\,\text{V}$ (NOT 0 V)).
   - **TEST SWITCHES BEFORE CONNECTING TO** CLK **and** $\overline{CLK}$.
     - Construct the testing circuit shown below.
       - Connect V_{DD} (+) and V_{SS} (−).
       - Connect *input* of one switch to V_{DD} (+) through a 1 kΩ resistor.
       - Connect *output* of switch to 0 V (*not* V_{SS}) through a 1 kΩ resistor.
       - To *open* switch, connect its *control* to V_{SS} (−) through a 1 kΩ resistor (for safety).
         - Use DMM to verify switch *input* sees V_{DD} and switch *output* sees 0 V.
       - To *close* switch, **RE**connect its *control* to V_{DD} (+) (again, through a 1 kΩ resistor).
         - Use DMM to verify switch *input* **and** *output* both see ***SAME*** $V_{DD}/2$.
       - **RE**connect *control* to CLK to verify (with oscilloscope) *no significant switch delay.*
     - Repeat until you find **two** working switches. Only get a new chip if 3+ switches fail.



CONTROL Z	$\Longrightarrow$	I	O
V_{SS} (−)	$\Longrightarrow$	V_{DD}	0 V
V_{DD} (+)	$\Longrightarrow$	$V_{DD}/2$	$V_{DD}/2$

- Disconnect testing setup (i.e., remove 1 kΩ resistors from input, output, and control pins).
- Connect V_{DD} (+) and V_{SS} (−).
- Connect CLK to *control* pin for one switch (switch S_1).
- Connect $\overline{CLK}$ to *control* pin for other switch (switch S_2).

4. **Convert continuous-time integrator** by replacing 10 kΩ resistor with switched capacitor.
   - Use same LF351 operational amplifier from before.
     - Use same supply rails: ±6 V (at *least*)
     - Same feedback capacitor: 0.01 μF (capacitor code: `103`).
     - Again, **to help with offset**, connect non-inverting input (i.e., "+" input) to ground via a 10 kΩ (variable) resistor (i.e., instead of a direct short-circuit connection).
   - Use Equation 2.6 (from book) with $f_{CLK} = 100$ kHz to **calculate** C_1 for 10 kΩ equivalent resistance.
   - Connect components as in Figure 2.9 in lab book.
     - Note that capacitor C_1 tied to **ground** (i.e., 0 V).
5. Test integrator with same 0-offset square wave input as before.
   - Output should be very similar to continuous-time integrator output. Again, **find its slope**.
     - Additional clock noise will make output "spikey."
     - Auto-scaling features of oscilloscope may not work.
     - Relatively large *bypass capacitors* on power rails may reduce *some* output noise.
     - `Average` feature in scope's `Acquire` settings may help.
     - It's possible that the down-going slope may be **curved.** If so, focus on up-going slope.
     - **Clipping and offset**: Try same strategies as before.
       - Double-check input signal amplitude (2.5 V) and offset (0 μV_{DC}).
       - Adjust value of non-inverting input (i.e., "+" input) resistor to ground.
       - Adjust input signal offset.
       - Adjust supply rails.
6. **SAVE A PLOT** that shows both the input and output on the same screen.
   - In this plot, show effect of clock-induced noise (i.e., do **not** use oscilloscope averaging).
7. **SAVE AN *AVERAGED* PLOT** that shows both the input and output on the same screen.
   - Use oscilloscope's `Average` under `Acquire` to clean up plot.
   - Position `Cursors` to measure ΔY and ΔX so you can calculate triangle wave slope.
   - Save the plot **with slope cursors shown**.

In your report, discuss the similarities and differences between the outputs and operation of the two integrators.