ECE 327: *Electronic Devices and Circuits Laboratory I*

Notes for Lab 2 (Field Effect Transistor Lab)

1. Trans-istor: <u>trans</u>**conductance** (variable) res<u>istor</u>

   - Bipolar ("accident") and unipolar (FET, "valve", like "tube") varieties
     - New technologies share features of both (e.g., insulated gate bipolar transistors (IGBTs))
   - **Voltage**-controlled current sources (VCCS)
     - Vary *channel resistance* in order to make current constant
     - Think of "transistor man" from Horowitz and Hill (1989)
   - For a bipolar transistor, base–emitter diode is forward biased, so it carries current too. So

     $$i_B = I_S \left(\exp\left(\frac{v_{BE}}{kT/q} \right) - 1 \right) \qquad \text{where } \frac{kT}{q} \approx 25.3\,\text{mV @ room temperature}$$

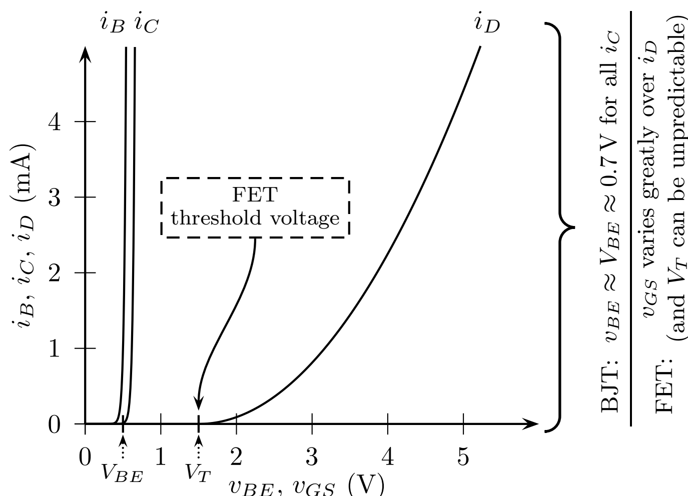
     and

     $$i_C = \beta I_S \left(\exp\left(\frac{v_{BE}}{kT/q} \right) - 1 \right) = \beta i_B$$

     where $I_S \approx 0$ and $\beta \gg 1$ are determined by material properties. Fortunately, $i_C = \beta i_B$. This relationship and the (steep) exponential i–v curves help make the bipolar transistor so handy.
   - For a unipolar transistor (FET), no current enters the gate. So $i_G = 0$ and

     $$i_D = K \left(v_{GS} - V_T \right)^2$$

     where $0.5\,\text{V} < V_T < 10\,\text{V}$ and (small) K are determined by material properties and temperature.
   - Graphically:



     - Notice vertical scale. Consider v_{GS} required for a *significant* drain current
     - Additionally, threshold V_T can have a 5 V manufacturing spread (!!)
     - NOTE: In tiny region below V_T, unipolar has steep exponential curve similar to bipolar
   - BJTs: high transconductance (+), very non-linear curve (−), *predictable* base–emitter drop (+?)

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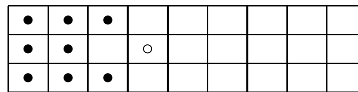
2. Analogous operation modes (gate ∼ base, source ∼ emitter, drain ∼ collector):

Condition	$\Longrightarrow$	Unipolar (FET)	∼	Bipolar (BJT)
Low gate–source voltage	$\Longrightarrow$	"Subthreshold"	∼	"Cutoff"
High gate–source voltage	$\Longrightarrow$	"Pinch-off" (or "Saturation")	∼	"Active"
Low source–drain voltage	$\Longrightarrow$	"Linear" (or "Triode" or "Ohmic")	∼	"Saturation"

- Bipolar and unipolar "saturation" are different (BJT: out of active mode, FET: into active mode)
- BJT "Saturation" versus FET "Ohmic" — only FETs can really be switches
  - Bipolar saturation is not practically usable (slow to exit, and can be impossible to use on IC)
  - In "Ohmic" mode, FET is like programmable resistor (e.g., electronic volume control, switches)

3. Diffusion reminder (demonstration: cold H_2O, hot H_2O, shaken H_2O, tilted H_2O (like diode))

- Diffusion is a statistical certainty (entropy increases)
  - Thermal agitation causes movement, but eventually "now" and "later" *look* identical
  - Movement is random, so clusters tend to spread out (i.e., "down" "diffusion gradient")



If the ○ is about to move or swap with a •, there is only a 1/8 chance that the result will be *more* concentrated. *Statistically* speaking, "order" tends to decrease (2nd law of thermodynamics).

4. Doping and the *pn*-junction

- Semiconductors are defined by their electron energies (not the same as "quasi-conductors")
  - Empty conduction band (no "free" carriers in structure)
  - Small "band gap" between valence and conduction bands
  - Small excitation energy (e.g., heat) lets electrons move to conduction band (become mobile)
- Semiconductor lattices and doping
  - Covalent bonds (silicon has four)
  - Can insert impurities by "doping"
    * *Neutral* atom with one less bonding electron inserts a "hole" in lattice
    * *Neutral* atom with one more bonding electron
  - Extra electrons and holes *can move* through lattice (like positive and negative carriers)
    * A semiconductor with lots of extra holes is "p"-type because holes *repel* from "positive"
    * A semiconductor with lots of extra electrons is "n"-type because electrons are "negative"
  - Because there are always the same number of *protons* and *electrons*, the material is always *NEUTRAL*; however, *SPACE CHARGE* can develop as impurities move
- The *pn*-junction and the diode "rectifier" (like *ball check valve*)
  - Join a *p*-type material and an *n*-type material to setup *diffusion gradient*
    * Holes from *p*-type will diffuse into *n*-type
    * Electrons from *n*-type will diffuse into *p*-type
  - Electric field builds up that stops diffusion (like weighted marbles tilting a balanced see-saw)
    * Extra holes in *n*-type setup a positive charge, which repels additional holes
    * Extra electrons in *p*-type setup a negative charge, which repels additional electrons
  - By applying enough *opposing* field (i.e., apply positive to *p* side), **bipolar** diffusion will continue (like rebalancing the see-saw) — ***bipolar*** **current** from **holes** *AND* **electrons**!
    * Temperature-dependent "diode drop" (0.6–0.7 V at 300 K) is diffusion *barrier* energy

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5. Bipolar (junction) transistor (BJT) device operation: **DIFFUSION** and *not* drift!
    - Opposing *pn* junctions (diodes) in series (*npn* ≈ *np*–*pn* and *pnp* ≈ *pn*–*np*)
        - Forward bias base–emitter diode by ∼0.7 V causes **bipolar** *diffusion* of electrons **AND** holes
        - Reverse bias base–collector diode
        - Diffusion is a current *source* — New carriers in base from emitter must go somewhere
            * Active mode: When base–collector diode reverse biased, carriers are *collected* and exit
            * Saturation mode: Otherwise, exit from *base*; extra current causes 0.8 V base–emitter drop
        - Asymmetric: Emitter and collector have same *type* of doping, but different amount/size/shape
        - Diffusion current proportional to emitter–base junction area
    - *Very* fast
        - New special versions (HBTs) operate at terahertz (THz) frequencies
        - For comparison, visible light starts around 750 THz
    - Price of bipolar:
        - Relatively high base current ("leakage")
            * High input (base) current drive makes simple BJTs impractical for power applications
        - BJT size is practically limited (i.e., BJTs are "large" on a piece of silicon — costly)

6. Unipolar or *field effect* transistor (FET): **DRIFT** and *not* diffusion!
    - In these devices, current flows through a conductive channel
        - Device is (principally) *symmetric*
        - *Source* and *drain* are ends of the channel
        - *Source* ≈ *emitter* and *drain* ≈ *collector*
            * For *n*-channel devices, "source" means more-**N**egative end (it *sources* electrons)
            * For *p*-channel devices, "source" means more-**P**ositive end (it *sources* holes/*sinks* electrons)
    - *Shape* of this channel can be changed by using a *field* to re-orient the charge carriers
        - Control voltage applied to a central *gate* (similar to "base")
        - Device acts like a *valve*
        - Similar to vacuum tube (grid ∼ gate, drain ∼ plate, source ∼ cathode/filament)
    - Voltage increases cross-sectional *area* of channel, so we expect squared v–i relationship (quadratic)
    - FET vs BJT:
        - very high input impedance (low leakage) (+), much smaller footprint/scalable/cheaper (+)
        - high input capacitance (−), slow (−)
    - The *Junction* FET (JFET): A depletion-mode device
        - A diode (*pn*-junction) "on its side" (symbol, often symmetric, looks like sideways diode)
            * Symbol depicts channel type (p/n); arrow is a "diode" that points toward n of *pn*-junction
            * "Diode" should always be reverse biased; amount of bias determines channel shape
        - Channel is shaped by reverse bias
            * If drop across channel is low, channel acts as resistance controlled by reverse bias
            * If drop across channel is high, channel gets triangular, and current "pinches off"
        - "Pinch off" mode acts as current source by *preventing* additional current
            * By Ohm's law, any more current would create a greater drop across channel
            * The additional reverse bias at drain side of channel would cut-off current completely
            * So expect an equilibrium current
            * Changing channel cross-section with gate voltage changes equilibrium current
        - A JFET channel exists until reverse bias takes it away; they're "depletion-mode" devices
            * Current flows "normally" (with gate–source shorted)
            * By applying field, we "deplete" the channel to turn current *off*
        - Relative to MOSFETs, JFETs are fast but have high leakage (< 100 pA)

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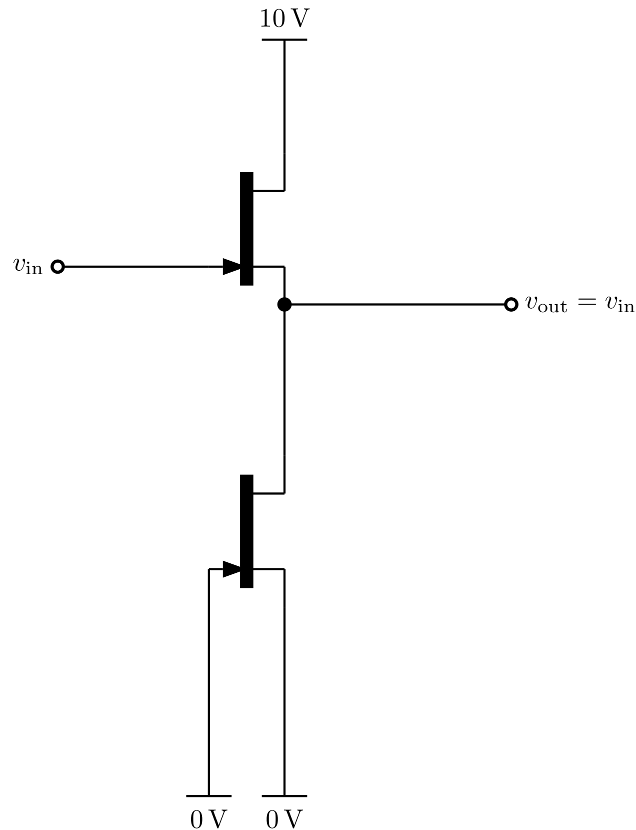

Figure L2-1: JFET source follower using matched JFETs.

- Clever example: JFET source follower in Figure L2-1
  - JFETs must be matched on the same piece of silicon
  - Both JFETs are depletion-mode devices
  - Bottom JFET is a current source (pinched-off channel at maximum size)
  - Same current flows through top JFET, so its gate and source differ by the same as the bottom gate and source
  - **Hence, the output follows the input *exactly* (no diode drops!)**

  - Reminder: Followers are used as voltage buffers
  - For a wide range of output currents, the output voltage stays the same
  - In other words, the output has *very low impedance* ($\Delta V/\Delta I \approx 0$; think Thévinin)

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7. Metal-Oxide-Semiconductor FET (MOSFET) or Insulated-Gate FET (IGFET)
   - Look like symmetric BJT
     - n-channel: two $n+$ regions separated by a p region
     - p-channel: two $p+$ regions separated by an n region
   - Middle region is "bulk" or "body"
     - Bulk–source junction must be reverse biased
     - Common (e.g., in power applications) to short bulk to one end of channel
       - Forces that end of channel to be *source*
       - Introduces a diode between drain and source
       - *MUST* be sure to keep drain–source reverse biased
     - Otherwise, short bulk to appropriate DC *rail* (e.g., high for p-channel and low for n-channel)
       - No difference between source and drain
       - Bidirectional current: great for switching applications
   - "Gate" separated from bulk by oxide (rust, SiO_2) *insulator*
     - Gate-oxide-bulk form MOS capacitor (gate: **M**etal, insulator: **O**xide, bulk: **S**emiconductor)
     - **DIELECTRIC BREAKDOWN** of oxide is both fatal and easy to induce
     - Gate–bulk field controls channel
       - Pulls/pushes excess carriers from/to *both* drain and source
       - Eventually, bulk region near gate gets *inverted* to other type
       - For low drain–source drop, uniform channel acts as gate–controlled resistor
       - For high drain–source drop, triangular channel "pinches off" current at constant value
   - Enhancement and depletion varieties exist
     - Enhancement: add a field to turn *on* current
     - Depletion: add a field to turn *off* current
   - In ohmic mode, low channel resistance and bidirectionality makes them great *switches*!
   - In a small space (cheap!!), can mimic (e.g., switching, ohmic, etc.) all *larger* passive components
   - Standard symbol: Shows insulated gate (MOS capacitor)
     - Channel: dashed or solid
       - dashed: enhancement ("normally off")
       - solid: depletion ("normally on")
     - Arrow: Diode formed by channel
       - Points toward n region (channel or bulk)
   - Alternative symbol: BJT-like (n-channel is **n**ot pointing in; etc.)
     - Thick depletion channel; Thin enhancement channel
   - Alternative symbol: Digital "switch"
     - Logic high turns n-channel on
     - Logic low turns p-channel on (bubbled symbol)
     - All enhancement mode
   - Using MOSFETs and BJTs
     - Common-gate, common-drain, and common-source work like analogous BJT configurations
     - MOSFETs have high gate capacitance and are slow, but have negligible gate leakage ($< 10\,\text{pA}$)
     - Unlike BJT, can swing from rail to rail (no diode drops to worry about)
     - IC designers can control MOSFET properties by adjusting geometry and oxide capacitance

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8. Complementary or Complementary-Symmetry MOS (CMOS)
   - Use n-channel and p-channel MOSFETs together in exactly equal and opposite ways
   - Low-power device — high input impedance and no current in digital operation
   - Because of high gate capacitance, power becomes a problem at high frequencies (V^2Cf)
     - Modern microprocessors have high FET count, so have high capacitance
     - Modern microprocessors are very fast (for absolutely no good *technical* reason)
     - Easily hit 2 kW with 30 M transistors at 4 GHz (!!!!)
     - Trick: Lower V
9. **Example:** CA3130 (uncompensated) **BiMOS** operational amplifier — schematic from datasheet
   - Recall: Operational amplifier is differential amplifier with (nearly) *infinite gain*
     - CA3160 is identical, but has *internal* compensation capacitor for unity-gain stability
   - Combines BJTs and MOSFETs
     - FETs: Minimal input leakage; maximal "rail-to-rail" output swing
     - BJTs: Give very *high gain* and *high speed*
       - Notice common-emitter amplifier with *current source* at collector ("dynamic load")
       - Current source has high impedance ($\Delta I/\Delta V \approx 0$; think Thévenin)
       - Common-emitter gain is collector impedance divided by emitter impedance (∞/tiny $\approx \infty$)
     - Current source implemented with (Cascode configuration) MOSFET current mirror
       - **Cascode**: Common-source followed by common-gate (yes, cascOde, with an "o")
       - "**Cascode**" historically describes an "**casc**aded tri**ode**", an alternative to a "pentode"
         - Traditional "cascades" connect plate anode ("drain") to grid ("gate") to magnify gain.
         - A "cascode" "**casc**ades" a plate an**ode** ("drain") with a filament cath**ode** ("source").
       - Here, common-source sets current (by mirror) and common-gate buffers current
       - Prevents channel-length modulation (like BJT Early effect) and Miller effect
     - Output stage is **CMOS inverter** operated in linear range (i.e., as *class-A amplifier*)
     - **NOTE:** Gate-oxide protection diodes (breakdown harmlessly and short out static discharge)
10. Laboratory experience (CMOS inverter, integrator review, switched-capacitor integrator)
    - Be very careful with MOS parts!
      - MOS parts:
        - CD4007 (3 CMOS pairs), CD4066 (4 CMOS analog switches), CD4049 (6 CMOS inverters), CA3160 (compensated BiMOS operational amplifier)
      - Static discharge can fry gate oxide (i.e., dielectric breakdown)
      - Keep one hand on breadboard metal when other hand is installing MOS chip
      - **DO NOT** install chip when power is on!
      - **DO NOT** forget to wire-up power rails. In fact, **DO IT FIRST**!!!
        - Power on *circuit* **before** signal source; turn *off* **signal source** *before* powering off circuit.
      - When debugging problems, test parts in isolation
      - If one component on a part is not working, try a different component on the same part
    - Use handouts for guidance on particular circuits
      - Detailed laboratory procedures (and pin-outs)
      - Continuous-time integrator schematics and explanations
    - Follow lab *book* (detailed instructions in supplementary text)
    - **DO NOT** disassemble continuous-time integrator! It is used in the switched-capacitor circuit!
    - When taking plots, save as CSV or BMP (or snap a CLEAR picture)
      - Show units; label axes; identify waveforms (e.g., "input"); show horizontal/vertical divisions
      - In most cases, channel grounds should be shown

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